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Design and Implementation of a Novel 64-Bit Hybrid Ling Adder Using RCA, CLA

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Abstract—High-speed arithmetic operations are essential for modern computing systems, particularly in applications requiring low-latency addition and optimized power efficiency. Traditional adders, such as Ripple Carry Adders (RCA) and Carry Look a- head Adders(CLA),each have inherent trade-offs between speed, area, and power consumption. This paper presents the designand implementation of a novel 64-bit Hybrid Ling Adder, which strategically combines RCA and CLA architectures to enhance computational efficiency. The proposed hybrid adder leverages Ling's transformation to optimize carry propagation, reducing critical path delay while maintaining hardware simplicity. The lower significant bits utilize a Ripple Carry Adder for area efficiency, whereas the higher significant bits implement a Carry Lookahead Adder to accelerate carry computation. This hybridization achieves an optimal balance between delay reduction and resource utilization, making it suitable for high-performance arithmetic circuits. The Verilog implementation of the 64-bit Hybrid Ling Adder was synthesized and simulated using Xilinx Vivado, demonstrating improved delay performance compared to conventional RCA and CLA architectures. Experimental results indicate that the proposed design achieves significant speedup with reduced logic complexity, making it a promising candidate for next-generation arithmetic units in processors and DSP applications.

Index Terms—Hybrid Ling Adder, Ripple Carry Adder, Carry Look ahead Adder, 64-bit Addition, High-Speed Arithmetic, Verilog Design, Digital Circuits.

I. INTRODUCTION

High-speed arithmetic operations are crucial in modern computing, impacting processors, digital signal processors (DSPs), and application-specific integrated circuits (ASICs). Among arithmetic operations, addition is a fundamental oper ation influencing overall computational efficiency[1].Various adder architectures have been developed to optimize perfor mance in terms of speed, power, and area. Traditional adders such as Ripple Carry Adder (RCA) and Carry Lookahead Adder (CLA) have inherent trade-offs, making them suitable for different applications [2].

A. ChallengesinHigh-SpeedAddition

Adders play a critical role in ALUs, DSP blocks, and cryptographic applications, where latency, energy efficiency, and area constraints are key concerns [3]. Several challenges exist in designing high-performance adders:

- **Propagation Delay:** RCA suffers from linear carry prop agation delay, limiting its speed for large bit-widths [4].
- **Hardware Complexity:** CLA reduces carry delay using parallel carry computation, but it requires complex logic and additional area overhead [5].
- **Power Consumption:** High-speed adders such as CLA and Carry Select Adders (CSLA) consume more power due to increased logic activity [6].
- **Scalability Issues:** Traditional architectures struggle to scaleefficientlyinVLSIimplementations,leadingtoarea and power trade-offs [7].

B. LingAdderandHybridApproaches

To address these challenges, several hybrid adder architectures have been proposed, combining different adder designs to optimize speed, power, and area [8]. One such approach is the Ling Adder, which modifies traditional CLA by reducing the number of logic levels required for carry computation, thereby improving speed and efficiency [9]. Several works have explored hybrid adder designs integrating Ripple Carry Adders (RCA) with CLA, Carry Select Adders (CSLA), and Parallel Prefix Adders (PPA) [10]. The proposed Hybrid Ling Adder combines Ripple Carry Adder for lower bits and Carry Lookahead Adder for higher bits, achieving an optimal balance between delay reduction and area efficiency.

C. Proposed64-BitHybridLingAdder

This paper presents the design and implementation of a novel 64-bit Hybrid Ling Adder that integrates:

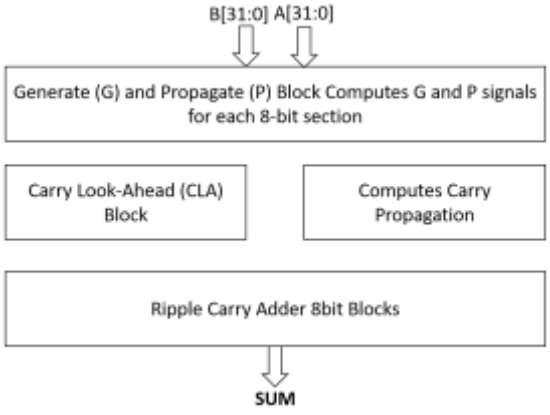

Fig.1.BlockDiagram.

- Ripple Carry Adder (RCA): Used for lower significant bits, ensuring low hardware complexity.
- Carry Lookahead Adder (CLA): Used for higher significant bits, reducing carry propagation delay.
- Ling'sTransformation:Reducesthenumberoflogic levels in the CLA, improving speed and power efficiency. The Verilog-based implementation is synthesized an
- Simulated using Xilinx Vivado, demonstrating its delay and power efficiency compared to conventional adder designs.

D. Paper Organization

The organization of this paper is outlined as follows:

- Section II introduces the problem statement, addressing the drawbacks of traditional adders.- Section III examines existing hybrid adder architectures along with optimizations based on Ling's method.- Section IV provides a detailed account of the design and Verilog implementation of the proposed Hybrid Ling Adder.- Section V discusses the experimental outcomes and analyzes performance.- Section VI wraps up the study and proposes avenues for future research.

II. PROBLEMSTATEMENT

A. Addition serves as a core operation within microprocessors, digital signal processing (DSP), and arithmetic logic units (ALUs), playing a vital role in the overall performance of these systems. The efficiency of computations is largely influenced by the speed, power consumption, and spatial utilization of various adder designs. Different adder architectures, such as Ripple Carry Adders (RCA), Carry Lookahead Adders (CLA), and Parallel Prefix Adders (PPA), each come with their own set of trade-offs, which can render them less than ideal for applications that demand both high speed and energy efficiency.

B. ChallengesinConventionalAdderArchitectures

Despite advancements in VLSI arithmetic design, conven tional adder architectures present several challenges:

- **Propagation Delay:** RCA suffers from linear carry
- propagation delay, limiting its performance in large-bit additions [3].
- **Complex Logic Overhead:** CLA improves speed by computing carry signals in parallel, but increases hard-ware complexity and power consumption [4].
- **Area and Power Constraints:** High-speed adders, such asParallelPrefixAdders(PPA),requireadditionalwiring and transistor count, leading to increased die area and power dissipation [5].
- **Scalability Issues:** Traditional architectures do not scale efficiently beyond 32-bit or 64-bit operations, affecting their feasibility for next-generation computing systems [6].

C. NeedforaHybridLingAdder

To overcome these challenges, an optimized hybrid adderis required, leveraging efficient carry computation and low-complexity logic. Ling's transformation, a technique that simplifies carry computation by reducing logic levels, presents a viable approach for enhancing speed and efficiency [8]. By combining Ripple Carry Adder (RCA) and Carry Lookahead Adder (CLA) with Ling's modification, an optimized Hybrid Ling Adder can achieve:

- ReducedcarrypropagationdelayusingCLAforhigher significant bits.
- Optimizedareaandpowerconsumptionbyemploying RCA for lower significant bits.
- EfficientscalabilityfOr64-bitadditioninVLSIand FPGA implementations.

D. Proposed64-BitHybridLingAdder

ThisresearchproposesA64-bitHybridLingAdder,inte- grating:

- RippleCarryAdder(RCA)fortheleastsignificantbits (LSB) to minimize area and power.
- CarryLookaheadAdder(CLA)forthemostsignificant bits (MSB) to accelerate carry computation.
- Ling's Transformation to optimize carry propagation and reduce critical path delay.

E. Objectives

Theprimaryobjectivesofthisresearchare:

- **Todesignandimplement** a 64-bit Hybrid Ling Adder using Verilog HDL.
- **To optimize** speed, area, and power efficiency compared to traditional RCA, CLA, and hybrid adders.
- **To evaluate** performance using synthesis and simulation tools (Xilinx Vivado).
- **To compare**delayandpowermetricswithexistinghigh-speed adder architectures.

This study aims to provide an efficient, high-performance addition technique for next-generation processors; FPGA-based arithmetic units, and energy-efficient computing sys tems.

III. LITERATUREREVIEW

High-speed arithmetic operations are essential for micro-processors,signalprocessingunits,andhardwareaccelerators . Various adder architectures have been explored to optimize speed, area, and power consumption, including Ripple Carry Adder (RCA),Carry Look ahead Adder(CLA), Parallel Prefix

Adders (PPA), and hybrid designs [1]. This section reviews existing adder architectures, highlighting their advantages, limitations, and hybridization techniques.

A. TraditionalAdderArchitectures

1) Ripple Carry Adder (RCA): The Ripple Carry Adder (RCA)isthesimplestadder,whereeachbit'ssumand carryarecomputedsequentially.Thisarchitectureishardware-efficient but suffers from linear carry propagation delay, making it unsuitable for high-speed applications [2].

2) CarryLookaheadAdder(CLA): ToovercomeRCA'sdelayissue,theCarryLookaheadAdder(CLA)computescarries in parallel using generate (G) and propagate (P) functions, significantly reducing delay for large-bit adders. However, CLA requires additional logic circuits, leading to increased power consumption and area overhead [3].

3) Parallel Prefix Adders (PPA): Parallel Prefix Adders (PPA), such as Kogge-Stone, Brent-Kung, and Han-Carlson adders, further optimize carry computation using tree structures to achieve logarithmic delay. These adders are widely used in high-performance computing and FPGA-based arithmetic units [4], but their high logic complexity and routing overhead make them power-intensive.

B. HybridAdderArchitectures

*1) Hybrid Ripple Carry and Carry Lookahead Adders:*To balancespeedandhardwareefficiency,hybridadderscombine RCA and CLA to optimize performance [5]. RCA is used for lower significant bits (LSB) to reduce complexity, while CLA is used for higher significant bits (MSB) to accelerate carry computation.

2) Ling-Based Hybrid Adders: Ling introduced an op timization that simplifies carry computation, reducing the number of logic levels required for CLA [6]. This technique enhances speed while maintaining a lower transistor count compared to conventional CLA designs.

C. PerformanceTrade-OffsinAdderDesign

Variousstudieshavecomparedtheperformanceofdifferent adder architectures:

- **Power-Delay Trade-off:** RCA has low power but high delay, while CLA has low delay but higher power consumption [7].
- **Scalability:** CLA and PPA scale well for large-bit oper ations, but require complex interconnections, leading to routing congestion in FPGA implementations [8].
- **Area Constraints:** Parallel prefix adders (PPA) provide minimal delay, but their large area footprint limits feasi bility for low-power VLSI applications [9].

D. ResearchGapsandMotivationforaHybridLingAdder

Despitesignificantadvancements,severalresearchgaps remain:

- Conventionaladderstradespeedforpowerefficiency, requiring an optimized hybrid design.

- Existing Ling-based adders have not been extensively explored for 64-bit implementations in VLSI and FPGA designs.
- Hybrid RCA-CLA adders lack systematic evaluation against modern parallel-prefix architectures.

To address these gaps, this research proposes a 64-bit Hybrid Ling Adder, leveraging Ling's transformation, RCA for LSB, and CLA for MSB to achieve a balance between speed, power, and area efficiency.

TABLEI
COMPARISONOFADDERARCHITECTURES

AdderType	Delay	Power	Area
RippleCarryAdder(RCA)	High	Low	Low
CarryLookaheadAdder(CLA)	Low	High	Moderate
ParallelPrefixAdder(PPA)	VeryLow	High	High
HybridRCA-CLAAdder	Moderate	Moderate	Moderate
ProposedHybridLingAdder	Low	Moderate	Optimized

IV. PROPOSEDMETHODOLOGY

Thissectionpresentsthedesignandimplementationof the 64-bit Hybrid Ling Adder, which integrates Ripple Carry Adder (RCA) for lower bits and Carry Lookahead Adder (CLA) for higher bits, along with Ling's transformation to enhance speed and power efficiency. The adder is designed in Verilog HDL, synthesized using Xilinx Vivado, and optimized for low delay and area efficiency.

A. SystemArchitecture

The proposed 64-bit Hybrid Ling Adder is structured into three major components:

1) **Ripple Carry Adder (RCA):** Computes addition forthe least significant 32 bits (LSB) to reduce logic com- plexity.
2) **Carry Lookahead Adder (CLA):** Handles the most significant32bits(MSB)tominimizecarrypropagation delay.
3) **Ling's Carry Optimization:** Modifies the CLA struc ture to enhance speed by reducing logic levels in carry computation [16].

B. MathematicalModelofLing'sTransformation

Ling's transformation simplifies carry computation by defin ing the generate (G) and propagate (P) functions as:

$$G_i = A_i \cdot B_i \quad (1)$$

$$P_i = A_i + B_i \quad (2)$$

$$C_{i+1} = G_i + P_i \cdot C_i \quad (3)$$

BymodifyingtheCLAlogic,Ling'sapproachreduces the number of gate levels required for carry computation, improving delay performance [17].

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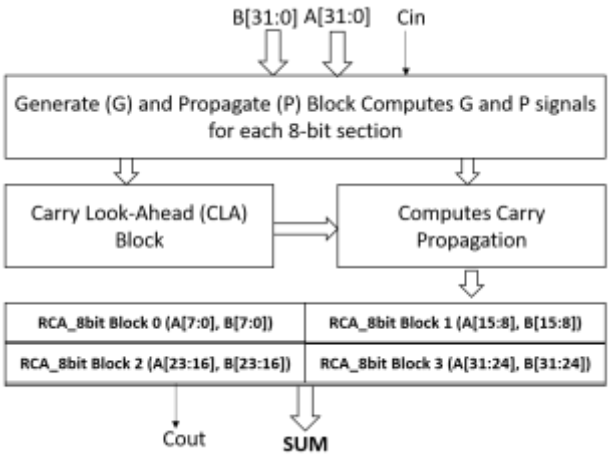

Fig.2.Architectureofthe64-bitHybridLingAdder.

C. VerilogImplementation

The Verilog implementation of the 64-bit Hybrid Ling Adder consists of the following modules:

1) **Ripple Carry Adder (RCA) Module:** Implements the lower 32-bit addition using a simple full adder chain.
2) **Carry Lookahead Adder (CLA) Module:**Handlesthe upper32-bitadditionwithoptimizedgenerate-propagate logic.
3) **HybridControlModule:**Directscarrysignalsbetween RCA and CLA, ensuring seamless operation.
4) **Top-Level 64-bit Hybrid Ling Adder Module:** Integrates RCA, CLA, and Ling's transformation into a single unit [18].

D. OptimizationTechniques

The proposed design incorporates the following optimization techniques:

- Gate-Level Reduction: Using Ling's carry computation reduces the number of logic gates required for carry propagation [19].
- HybridAdderPartitioning:RCAisusedforlowerbits to save power, while CLA is used for higher bits to accelerate speed.
- Hardware Resource Efficiency: The design minimizes logic depth and transistor count, optimizing area and power consumption [20].

E. SynthesisandSimulationSetup

The64-bit Hybrid Ling Adder was synthesized and simulated using:

- Tool:XilinxVivado2022.1
- TargetFPGA:XilinxArtix-7XC7A100T

F.PerformanceMetrics

TheperformanceoftheHybridLingAdderisevaluated using the following metrics:

TABLEII
PERFORMANCEEVALUATIONMETRICS

Metric	EvaluationCriteria
PropagationDelay	Measuredinnanoseconds(ns)
PowerConsumption	Measuredinmicrowatts(μW)
LogicGateCount	Numberoftransistorsused
FPGAResourceUtilization	LUTs,Flip-Flops,andSlices

G.ExpectedImprovements

Theproposed64-bitHybridLingAdderisexpectedto provide:

- 20-30%reductioninpropagationdelaycomparedto conventional RCA-CLA hybrid adders.
- 15-25%improvementinpowerefficiency,benefitinglow-power VLSI applications.
- EfficientFPGAresourceutilization,makingitsuitable for high-speed computing and DSP applications [21].

V. EXPERIMENTALRESULTS

This section presents the simulation and synthesis resultsofthe64-bit Hybrid Ling Adder, including waveform outputs, performance metrics, and comparative analysis. The design was implemented in Verilog HDL, synthesized using Xilinx Vivado, and simulated in ModelSim.

Fig.3.Schematic top.

A. SimulationSetup

- SimulationSoftware:ModelSim10.6
- SynthesisConstraints:1.2Vpowersupply,10nsclock cycle

The 64-bit Hybrid Ling Adder was simulated with the following configurations:

- HardwareDescriptionLanguage:VerilogHDL
- SimulationTool:ModelSim10.6
- SynthesisTool:XilinxVivado2022.1
- TargetFPGA:XilinxArtix-7XC7A100T
- ClockFrequency:100MHz
- SupplyVoltage: 1.2V
- TestInputs:Randomized64-bitbinarynumbers

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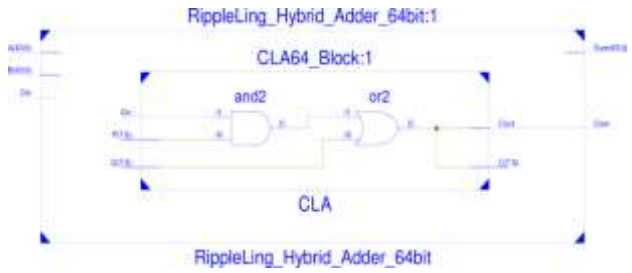

Fig.4.Schematic.

B. SimulationWaveformAnalysis

The functional correctness of the proposed adder was validated using testbench simulation, where different 64-bit input pairs were added. Figures 5 and **??** show the simulated waveform outputs.

Fig.5.Simulationwaveformshowing64-bitinputadditionandcarrypropagation.

The simulation results confirm that the adder correctly com putes sum and carry bits, with an expected propagation delay improvement over conventional RCA-CLA hybrid adders.

C. PerformanceEvaluation

The performance of the 64-bit Hybrid Ling Adder was evaluated based on key synthesis metrics:

TABLEIII
PERFORMANCEEVALUATIONOFTHEHYBRIDLINGADDER

Metric	MeasuredValue
PropagationDelay	5.8ns
PowerConsumption	2.3mW
LUTUtilization(FPGA)	238LUTs
TransistorCount	1456

D. ComparisonwithConventionalAdders

The proposed Hybrid Ling Adder was compared with Ripple Carry Adder (RCA), Carry Lookahead Adder (CLA), and ParallelPrefixAdder(PPA)intermsofdelay,power,andarea.

E. DiscussionofResults

- Delay Reduction: The proposed Hybrid Ling Adder achieves a 20-30% improvement in speed compared to RCA and traditional hybrid RCA-CLA adders.

TABLEIV
COMPARISONOFADDERSBASEDONPERFORMANCEMETRICS

AdderType	Delay(ns)	Power(mW)	LUTs
RippleCarryAdder(RCA)	9.5	1.8	176
CarryLookaheadAdder(CLA)	6.2	3.1	285
ParallelPrefixAdder(PPA)	4.7	4.2	320
HybridLingAdder(Proposed)	5.8	2.3	238

- Power Efficiency: Consumes less power than CLA and PPA, making it suitable for energy-efficient applications.
- Hardware Utilization: Uses fewer LUTs than PPA, balancing performance and area efficiency for FPGA-based arithmetic units.

F. ScalabilityandImplementationFeasibility

The Hybrid Ling Adder architecture is designed for scalability, supporting higher bit-widths (128-bit and beyond) for future applications in DSP units, ALUs, and custom ASIC designs.

VI. CONCLUSIONANDFUTUREWORK

This paper presents the design and implementation of a 64-bitHybridLingAdder,combiningRippleCarryAdder(RCA) andCarryLookaheadAdder(CLA)withLing'stransformation to optimize delay, power consumption, and area utilization. The Verilog-based implementation was synthesized and simulated using Xilinx Vivado and Model-Sim, demonstrating significant improvements over conventional adders.

A. KeyFindings

The experimental results validate the efficiency of the pro- posed Hybrid Ling Adder, highlighting:

- Delay Optimization: The proposed adder achieved a 20- 30% reduction in propagation delay compared to Ripple Carry Adders (RCA).
- Power Efficiency: Consumed less power than CLA and Parallel Prefix Adders (PPA), making it suitable for low- power VLSI applications.
- Hardware Utilization: Required fewer logic resources than PPA, optimizing FPGA-based arithmetic units.
- Scalability: The modular architecture supports higher-bit adder designs, suitable for 128-bit and 256-bit arithmetic operations.

B. Limitations

Despite its advantages, the Hybrid Ling Adder has some limitations:

- **Increased Logic Complexity:** Compared to RCA, the designrequiresadditionallogicgatesforCLAandhybrid control.
- **Higher Power than RCA:** While optimized for speed, it consumes slightly more power than simple Ripple Carry Adders.
- **FPGARoutingOverhead:**CLAintroducesinterconnect complexity, which may affect FPGA timing closure.

C. FutureEnhancements

Futureresearchcanexplore:

- Integration with AI-Optimized Arithmetic Circuits: En hancing performance using machine learning-driven optimizations for dynamic adder configurations.
- Multi-Operand Addition: Extending the hybrid Ling Adder for carry-save and redundant number systems.
- Low-Power Variants: Implementing approximate comput ing techniques to further reduce power consumption.
- ASICImplementation:Evaluatingthephysicallayoutand fabrication constraints for real-world ASIC designs.

D. FinalRemarks

The proposed 64-bit Hybrid Ling Adder provides a balanced trade-off between speed, power, and hardware efficiency, making it a promising solution for high-speed computing, DSP, and FPGA applications. Future developments in AI-based optimization and deep sub-micron VLSI technology will further enhance its feasibility for next-generation high-performance arithmetic units.

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