Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 10, October : 2024

PERFORMANCE ANALYSIS OF FIR FILTERS WITH PARALELL PREFIX ADDERS

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ABSTRACT

Typically, a DSP digital filter application uses an A/D converter to receive input samples, a D/A converter to perform the mathematical operations necessary to determine the filter type, and a D/A converter to output the result. This application uses mostly FIR filters. Analog filters are distinguished from digital filters by the fact that digital filters calculate the filter response using arithmetic with finite precision, while analog filters employ finite precision mathematics to describe signals. For the purpose of this project, a FIR filter is constructed in Xilinx ISE by making use of the dialect VERILOG. Within the scope of this project, VERILOG coding for the FIR filter is developed, and waveforms are examined using simulation.

The adders that have been selected for this project are the Kogge stone adder, the Sklansky adder fisher, and the Square root carry select adder with fisher. As part of this project, we are required to create a real-time language (RTL) for the structures, as well as validate the functioning of the structures and carry out the synthesis using a Xilinx synthesizer. A comparison is made between the outcomes in terms of speed for a number of different fir constructions.

Key words : FIR Filter ,KSA,SKA,BKA and Verilog HDL.

1.INTRODUCTION

Digital filters are used to a significant degree throughout the whole of the electronic sector. This is due to the fact that digital filters have the capability of achieving significantly higher signal-to-noise ratios than analog filters and At each intermediate transform step, the digital filter performs mathematical operations without producing any noise. while the analogue filter adds noise. For noise removal, spectrum structuring, and symbol interference elimination in communication infrastructures, digital filters are a powerful choice. Because of their perfect repeatability, These filters are popular because they allow design engineers to achieve performance levels that analogue filters cannot.

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Digital filters can be built using three math steps. Addition (or subtraction), multiplication (typically by a constant), and time delay (delaying a digital signal by one or more sample periods) follow. Figure 1 depicts a digital filter. The mathematical operations explained before can be used to define the filter's behaviour.

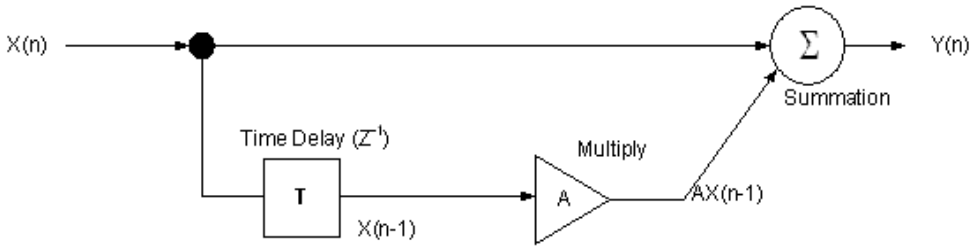

Figure 1. Block diagram of a Simple Digital Filter

The Impulse Response (int(n)) is the result of a digital filter receiving an input of the unit impulse function (δ(n)). It is possible to calculate the system response for any input sequence x(n) if the system's impulse response is known. The unit impulse is applied to a system at sample index n=0 in its prescribed form. Hence, h(n) is zero when n is less than zero since the impulse response is only non-zero when n is greater than or equal to zero. This impulse reaction is considered to be causal since, in the absence of this attribute, the system would be generating a response prior to the application of an input. A Linear Time Invariant System's reaction to a delayed unit impulse δ(n-k) is a delayed version of the unit impulse, indicated as h(n-k), based on its time-invariance property. The linearity property states that a system's response to a weighted sum of inputs is the total of its responses to each input. This is simultaneously known. A system's reaction to an arbitrary input x(n) can be stated as follows:

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k)$$

2.LITERATURE REVIEW

Researchers S. D. S. M. Mehendale and G. Venkatesh published an article titled "Synthesis of multiplier-less FIR filters with minimum number of additions." The use of digital filters is becoming more widespread in the music industry. Consequently, the implementation of a high-quality digital filter should be considered an essential component in the conception of audio system applications. Precision with restricted in digital filters for signal communication is different from simple filters like computerised filters that employ limited exactness number juggling to capture filter response. The FIR-filter was built in Xilinx ISE using VERILOG. VERILOG coding for the FIR-filter has been implemented, and waveforms may be observed in the reproduction.Viper is a more lightweight component in comparison to multipliers in terms of

silicon territory, and this is a factor that contributes to its financial success in the FIR system. In this particular piece of writing, multipliers have been selected as stall and Wallace, and adders have been included as convey spare and convey skip. As part of this study, it is necessary to construct a real-time logic (RTL) for the purpose of structures, as well as to evaluate the effectiveness of structures in comparison to one another and to perform the union using a Xilinx synthesizer. When considering the results, several fir structures were taken into consideration with relation to region (LUTs), power, deferral, and memory values.

3.FIR FILTERS USING VARIOUS ADDERS

A.FIR FILTERS USING KOGGE STONE ADDER

Implementing almost any kind of digital frequency response may be accomplished with the help of a FIR filter. In order to generate the output of the filter, these filters are often constructed using a multiplier, adders, and a sequence of delays. There was a multiplier that was used in traditional FIR filters for the purpose of multiplying the fixed coefficients in the FIR filter with the input data. For the purpose of adding the output from, the Kogge stone adder was used. To illustrate the fundamental FIR filter diagram of N length, the following graphic is shown. All of the input samples are affected by the outcome of the delays. During the process of multiplication, the coefficients that are used are the values of bi, where i = 1, 2, 3, etc. In order to ensure that the o/p at a time is calculated, which is the total of all the delayed samples multiplied by the proper factors.

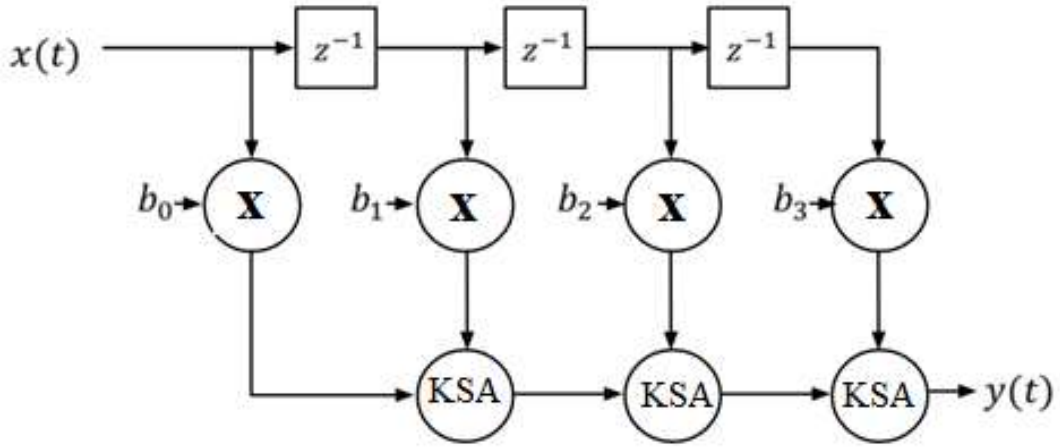

Figure 2. Logical Structure of FIR Filter using kogge stone adder

KOGGE STONE ADDER

KSA is a parallel prefix form carry look ahead adder. It is widely used in high-performance arithmetic circuits and is considered the fastest adder. It produces carry in O (logn) time, and both of these characteristics are widespread. Carry computations are performed

quickly in the Kingdom of Saudi Arabia (KSA) by processing them in parallel, although at the expense of larger space.

In order to have a comprehensive understanding of the operation of KSA, it is possible to analyze it in terms of three main categories:

1. Pre processing

This stage comprises calculation of produce and propagate signals matching too each pair of bits in A and B.

$$pi = Ai \; xor \; Bi$$

$$gi = Ai \; and \; Bi$$

2 . Carry look ahead network

The KSA adder is distinguished from other adders by this block, which is also the primary factor responsible for its exceptional performance rates. In this stage, the calculation of the carries that correspond to each bit is performed. It employs group propagate and produce as intermediary signals in its operation.

$$Pi{:}j = Pi{:}k{+}1 \; and \; Pk{:}j$$

$$Gi{:}j = Gi{:}k{+}1 \; or \; (Pi{:}k{+}1 \; and \; Gk{:}j \;)$$

3. Post processing

This is the last phase, and it is something that has been done by all of the adders in this family (carry look forward). For this purpose, calculation of sum bits is required.

$Si = pi \text{ xor } Ci\text{-}1$

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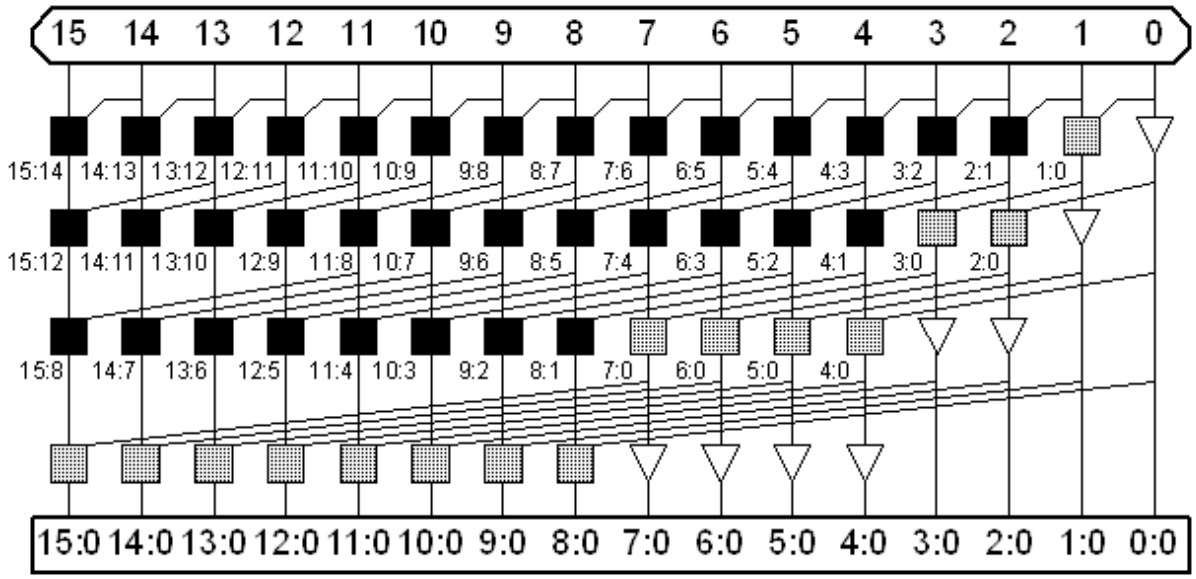

Figure 3. 16 bit kogge stone adder

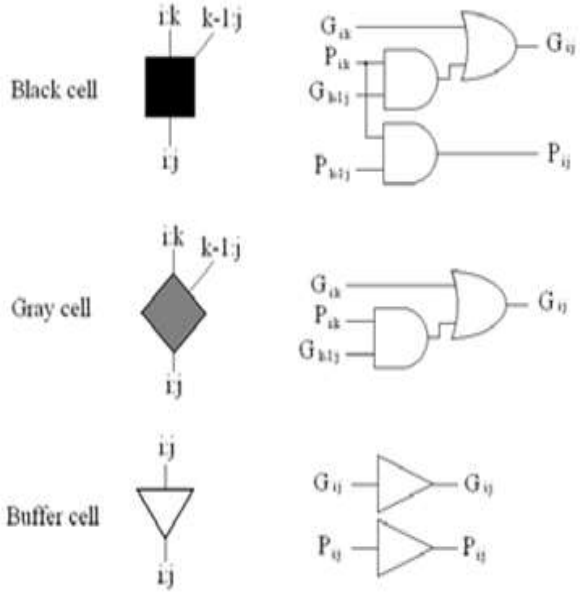

Figure 4. Complex logic cells inside the Prefix Carry Tree

B.FIR FILTERS USING SKLANSKY ADDER

Implementing almost any kind of digital frequency response may be accomplished with the help of a FIR filter. In order to generate the output of the filter, these filters are often constructed using a multiplier, adders, and a sequence of delays. There was a multiplier that was used in traditional FIR filters for the purpose of multiplying the fixed coefficients in the FIR filter with the input data. A sklansky adder was used in order to include the output from. To

illustrate the fundamental FIR filter diagram of N length, the following graphic is shown. All of the input samples are affected by the outcome of the delays. During the process of multiplication, the coefficients that are used are the values of bi, where i = 1, 2, 3, etc. To determine the o/p at a moment, multiply all delayed samples by the proper factors.

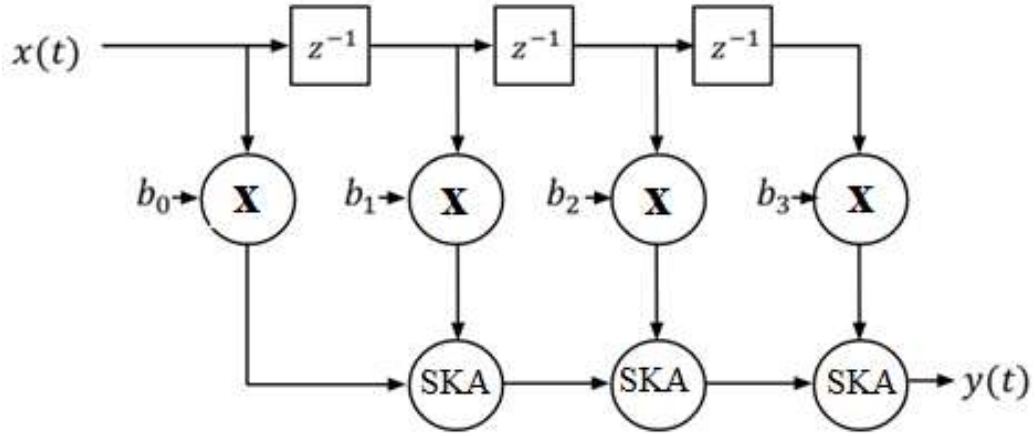

Figure5. FIR filter using skalansky adder

SKALANSKY ADDER

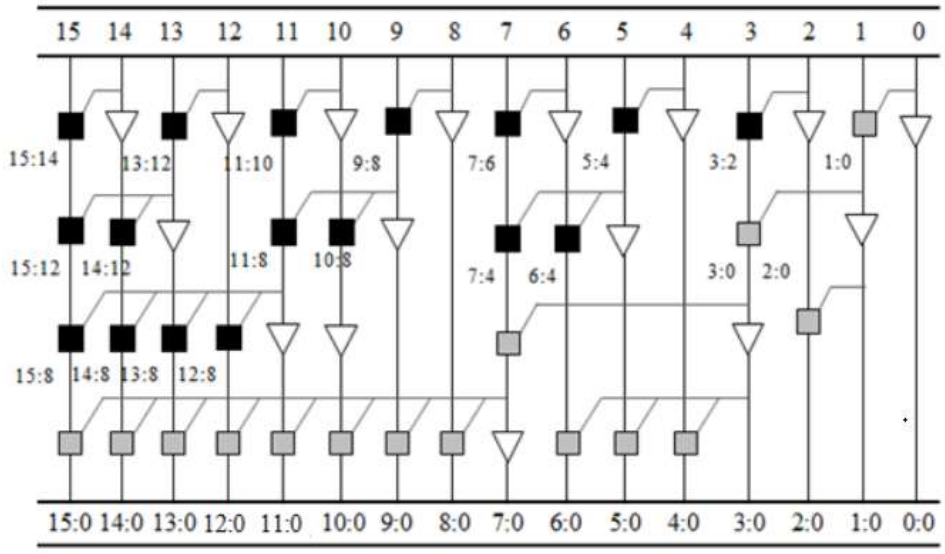

Figure 6. 16 bit skalansky adder

Presented below is a schematic representation of a 16-bit Sklansky adder. The Sklansky adder is similar to the divide-and-conquer tree in certain contexts. For the purpose of prefix addition, the conditional sum addition logic that was presented by Sklansky in 1960 provides a

minimal depth prefix network; however, this comes at the expense of higher fan-out for particular calculation nodes. At a node, the lateral fanning wires that are the longest extend to a total of two additional nodes. A substantial amount of delay is caused by the fact that the fan-out of the Sklansky's adder grows dramatically from the inputs to the outputs along the crucial route. The performance of the structure suffers as a result of this when the number of bits in the adder increases to a significant percentage.

C.FIR FILTERS USING SQUARE ROOT CARRY SELECT ADDER

Implementing almost any kind of digital frequency response may be accomplished with the help of a FIR filter. In order to generate the output of the filter, these filters are often constructed using a multiplier, adders, and a sequence of delays. There was a multiplier that was used in traditional FIR filters for the purpose of multiplying the fixed coefficients in the FIR filter with the input data. For the purpose of adding the output from, the square root carry choose adder was used. To illustrate the fundamental FIR filter diagram of N length, the following graphic is shown. All of the input samples are affected by the outcome of the delays. During the process of multiplication, the coefficients that are used are the values of bi, where i = 1, 2, 3, etc. To ensure that the o/p at a time is calculated, multiply all delayed samples by the necessary factors.

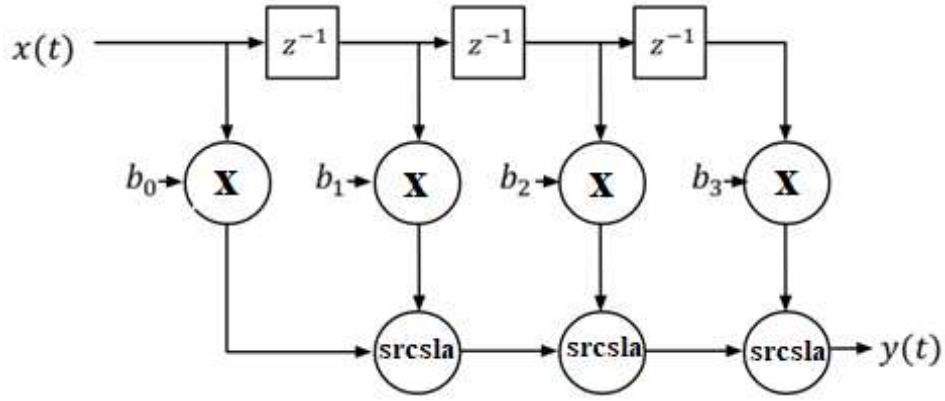

Figure7. FIR filter using SRCSLA

SQUARE ROOT CARRY SELECT ADDER (SRCSA)

Industrial Engineering Journal
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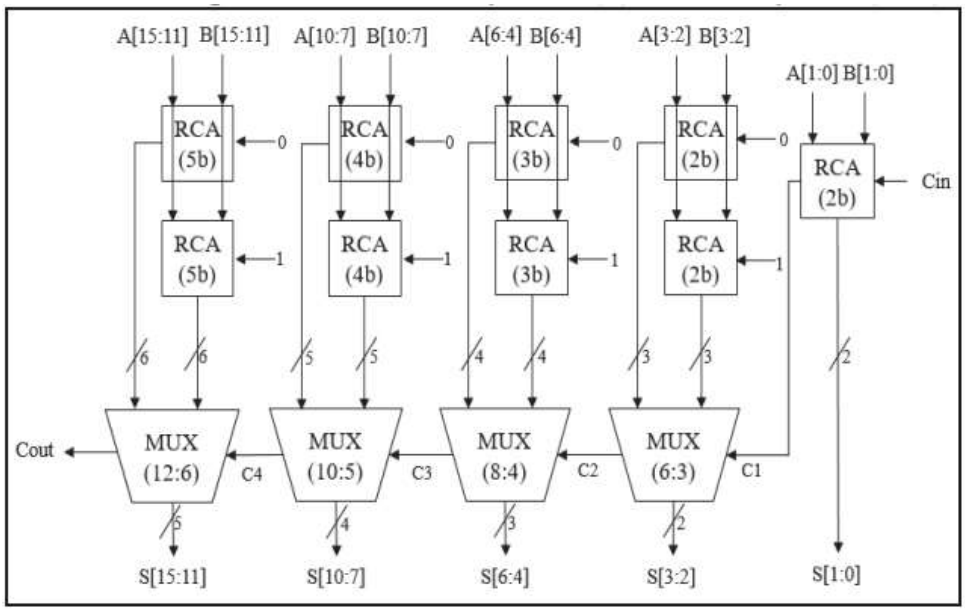

Figure 8. 16-bit SRCSA (proposed adder)

SRCSA, which stands for Square Root Carry Select Adder, allows for the block size to be controlled in a changeable manner. For the sake of brevity, the whole analysis is not shown here; nonetheless, for example, a 16-bit adder may be constructed by using block sizes of 2-2-3-4-5 rather than the more common practice of employing a block size of four (as was done before). In situations when the delay of the Full-Adder is equivalent to the delay of the MUX, this break-up is optimal. The proposed SRCSA adder for 16 bits is shown in Figure 3 as a block diagram. The inputs are labeled as A and B, and the carry-in is represented by the symbol Cin. The outputs are represented by the symbols sum (S) and carry-out (Cout).

4.RESULTS

RTL SCHEMATIC:RTL stands for register transfer level, which is an abbreviation for the register transfer level schematic. This schematic represents the blueprint of the architecture and is used to check that the planned architecture is comparable to the ideal architecture that we are yet to construct.The coding language known as verilog.vhdl is used in order to transform the description or summary of the architecture into the functioning summary. This is accomplished via the utilization of the hdl language. The RTL schematic even includes a description of the internal connection blocks, which allows for more accurate analysis.The RTL schematic diagram of the intended architecture is shown in the figure that serves as the representation below.

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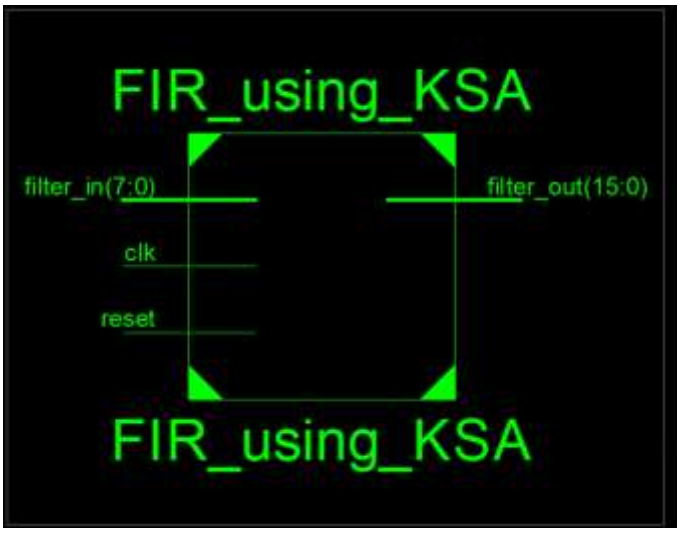

Figure 9. RTL Schematic of FIR filter using kogge stone adder

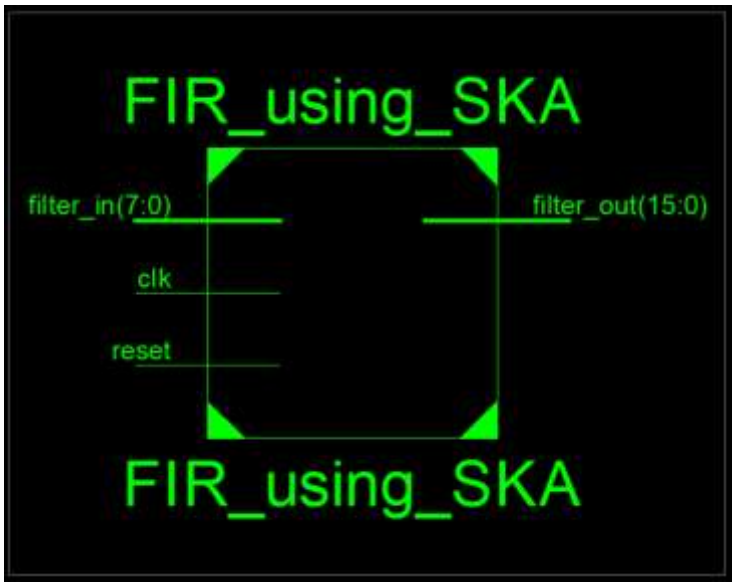

Figure 10. RTL Schematic of FIR filter using skalansky adder

Industrial Engineering Journal
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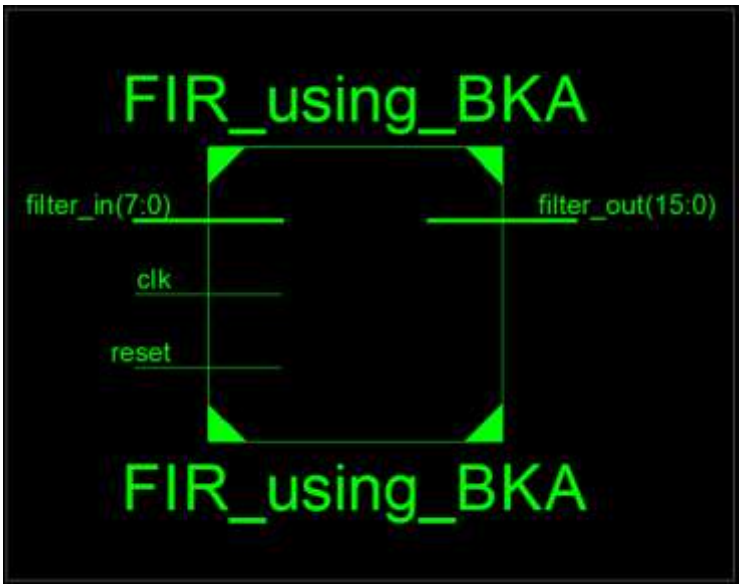

Figure11. RTL Schematic of FIR filter using brent kung adder

TECHNOLOGY SCHEMATIC: A representation of the architecture is created in the LUT format by the technology schematic. The LUT is considered to be the parameter of area that is used in VLSI for the purpose of estimating the design of the architecture.The LUT is considered to be a square unit, and the memory allocation of the code is physically reflected in the LUTs that are present in the FPGA.

Figure 12. View Technology Schematic of FIR filter using kogge stone adder

Figure 13. View Technology Schematic of FIR filter using skalansky adder

Figure 14. View Technology Schematic of FIR filter using brent kung adder

SIMULATION: As opposed to the schematic, which is the verification of the connections and blocks, the simulation is the procedure that is referred to as the ultimate verification in terms of

its functioning. During the process of transitioning from the implantation to the simulation on the main page of the tool, the simulation window is activated. The simulation window is responsible for containing the output in the form of wave shapes. For this purpose, it is able to provide a variety of radix number systems, which is a flexible feature.

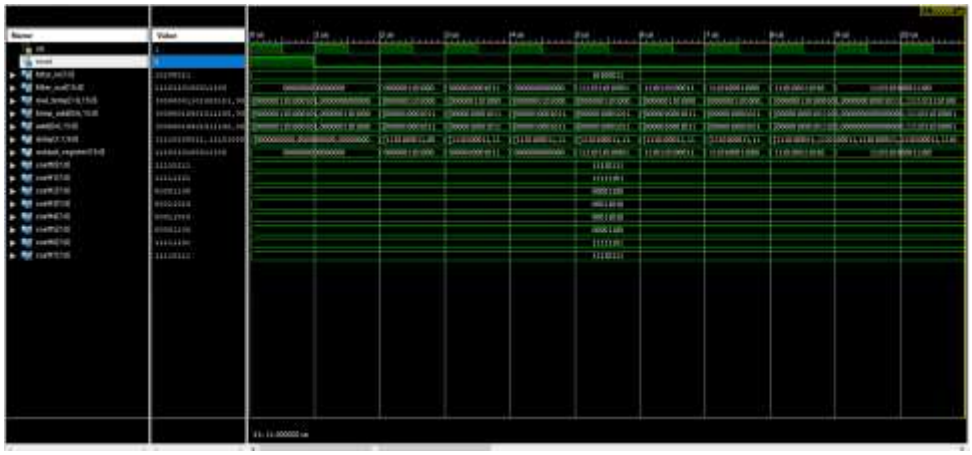

Figure15. Simulated Waveforms FIR filter kogge stone adder

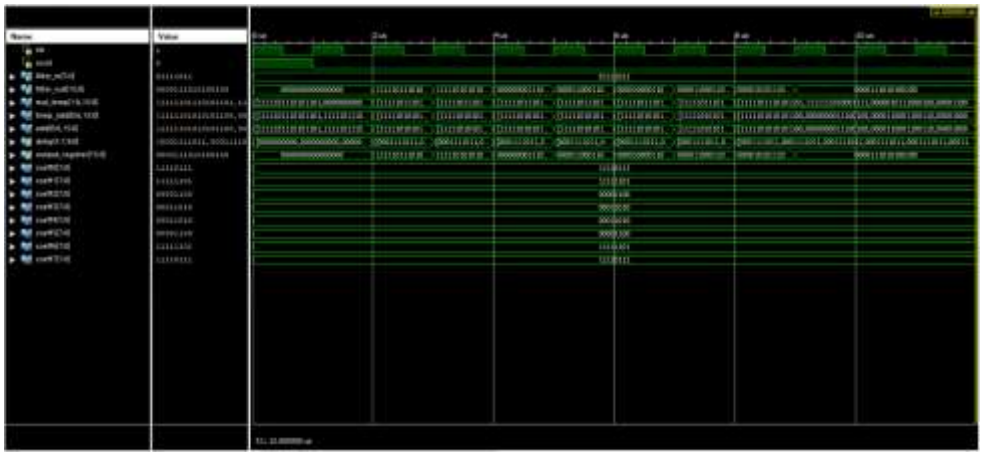

Figure16. Simulated Waveforms FIR filter skalansky adder

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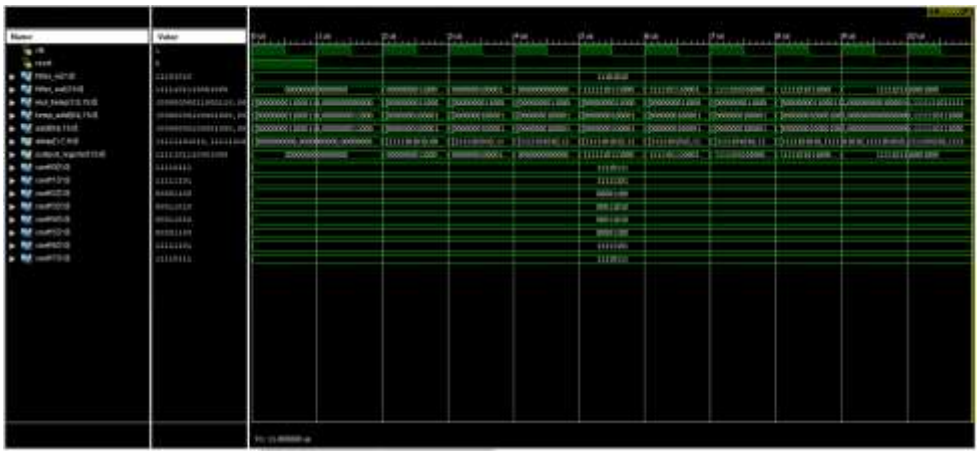

Figure17. Simulated Waveforms FIR filter brent kung adder

PARAMETERS: Taking into consideration that the characteristics that are handled in VLSI are area, delay, frequency, and power, one may assess the design of one architecture in comparison to another based on these criteria. Here, the consideration of area and frequency is being taken into account.

Parameter	FIR Using KSA	FIR Using SKA	FIR Using BKA
No of LUTs	528	347	320
Frequency (MHz)	122.234	121.374	128.584

Table1.parameter comparison

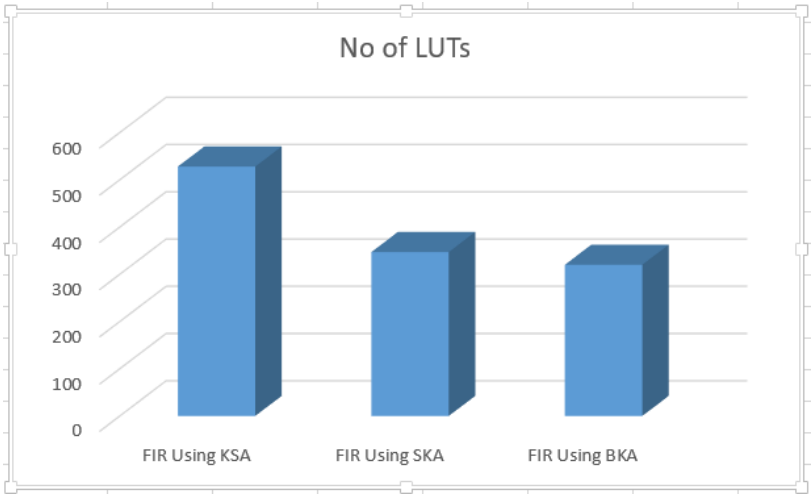

Figure18. LUT comparison bargraph

Industrial Engineering Journal
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Volume : 53, Issue 10, October : 2024

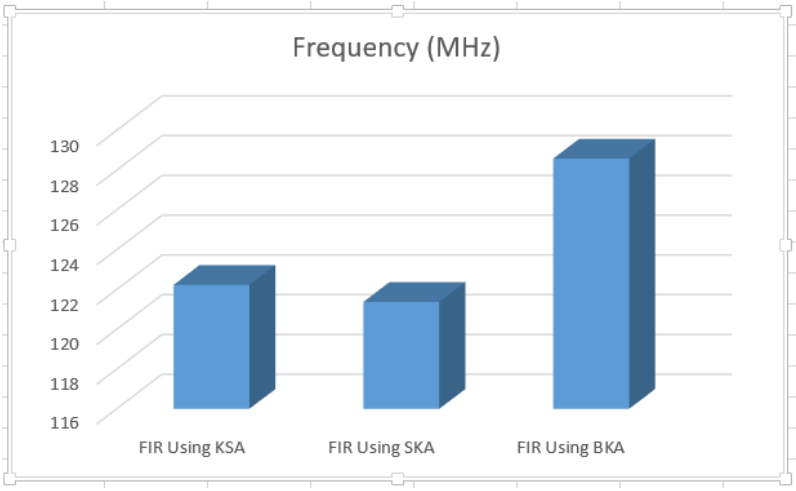

Figure19. frequency comparison bargraph

CONCLUSION

A great number different designs have been developed over the course of the last twenty years with the purpose of designing low-complexity fir operations. On the other hand, the FIR design does not exhibit such an improvement. That kind of demand may be satisfied by the project that is being discussed here. It is possible to draw the conclusion from the table that the FIR that uses the brent kung adder construction takes up less space and has a higher speed than the fir that uses the kogge stone Adder structure and the fir that uses the skalansky Adder structure. Therefore, as a result of this project, it has the opportunity to make use of the structure that corresponds to the needs of the industrial sector. It is possible that in the future, there will be an opportunity to improve these structures by using reversible logics in order to maximize the power in a slighter manner.

REFERENCES

[1] M. B. Gately, M. B. Yeary, and C. Y. Tang, “Multiple real-constant multiplication with improved cost model and greedy and optimal searches,” in Proc. IEEE ISCAS, May 2012, pp. 588–591.
[2] S. D. S. M. Mehendale and G. Venkatesh, “Synthesis of multiplier-less FIR filters with minimum number of additions,” in Proc. IEEE ICCAD,1995.
[3] L. Aksoy, C. Lazzari, E. Costa, P. Flores, and J. Monteiro, “Design of digit-serial FIR filters: Algorithms, architectures, and a CAD tool,” IEEE Trans. Very Large Scale Integration (VLSI) Syst., vol. 21, no. 3,pp. 498–511, Mar. 2013
[4] I. C. Park and H. J. Kang, “Digital filter synthesis based on minimal signed digit representation,” in Proc. Design Autom. Conf. (DAC),2001.

[5] Yu Pan and Pramod Kumar Meher, Senior Member, IEEE, “Bit-Level Optimization of Adder-Trees for Multiple Constant Multiplications for Efficient FIR Filter Implementation ,” Transactions On Circuits And Systems—I: Regular Projects, Vol. 61, No. 2, February 2014.
[6] R. Hartley and A. Casavant, “Tree-height minimization in pipelined architectures,” in Proc. IEEE ICCAD, Nov. 1989.
[7] M. Kumm, P. Zipf,M. Faust, and C.-H. Chang, “Pipelined adder graph optimization for high speed multiple constant multiplication,” in Proc.IEEE ISCAS, May 2012, pp. 49–52.
[8] D. R. Bull and D. H. Horrocks, “Primitive operator digital filter,” IEEE Proceedings-G, vol. 138, no. 3, pp. 401–412, Jun. 1991.
[9] Y. Voronenko and M. Püschel, “Multiplierless multiple constant multiplication,” ACM Trans. Algorithms, vol. 3, no. 2, 2007.
[10] A. G. Dempster and M. D. Macleod, “Use of minimum-adder multiplier blocks in FIR digital filters,” IEEE Trans. Circuits Syst. II, Analod Digit. Signal Process., vol. 42, no. 9, pp. 569–577, 1995.