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Enhanced and Power Optimized Fault Aware Stable SRAM Design

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ABSTRACT:

SRAM stability is a major concern in nanometer CMOS technologies. As the most important metrics of SRAM static stability, the static characteristics of SRAM are derived by static characteristic curves (read butterfly curve, standby butterfly curve, read N curve, write N curve and WNM curve). With the advancement of technology, the size of transistors and the distance between them are reducing rapidly. Therefore, the critical charge of sensitive nodes is reducing, making SRAM cells, used for aerospace applications, more vulnerable to soft-error. If a radiation particle strikes a sensitive node of the standard 6T SRAM cell, the stored data in the cell are flipped, causing a single-event upset (SEU). Therefore, in this paper, a Soft-Error-Aware Read-Stability-Enhanced Low- Power 12T (SARP12T) SRAM cell is proposed to mitigate SEUs. To analyze the relative performance of SARP12T, it is compared with other recently published soft-error-aware SRAM cells, QUCCE12T, QUATRO12T, RHD12T, RHPD12T and RSP14T. All the sensitive nodes of SARP12T can regain their data even if the node values are flipped due to a radiation strike. Furthermore, SARP12T can recover from the effect of singleevent multi-node upsets (SEMNUs) induced at its storage nodepair. Along with these advantages, the proposed cell exhibits the highest read stability, as the '0'-storing storage node, which is directly accessed by the bitline during read operation, can recover from any upset. Furthermore, SARP12T consumes the least hold power. SARP12T also exhibits higher write ability and shorter write delay than most of the comparison cells. All these improvements in the proposed cell are obtained by exhibiting only a slightly longer read delay and consuming slightly higher read and write energy.

***Index Terms*—Single-event upset (SEU), single-event multimode upsets (SEMNUs), critical charge, radiation hardness, read stability, hold power, write ability.**

INTRODUCTION:

By the analysis of Schmitt-Trigger (ST)- based differential- sensing static random access memory (SRAM) bit cells for ultralow-voltage operation, the ST-based SRAM bit cells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bit cell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bit cell. The proposed ST bit cells incorporate a built-in feedback mechanism, achieving process variation tolerance which is a must for future nanoscaled technology nodes. A detailed comparison of different bit cells shows that the ST-1 , ST-2 and proposed bit cell can operate at lower supply voltages. POrtable electronic devices

have extremely low power requirement to maximize the battery lifetime. Variousdevice-/circuit-/architectural-level techniques have been implemented to minimize the power consumption [1]. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly (to the first order) [1]. However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for SRAM bitcells employing minimum-sized transistors [2], [3]. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations.Intradie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell, resulting in asymmetrical characteristics [4]. The combined effect of the lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, writefailure, and access-time failure [4]. Moreover, it is predicted that embedded cache memories, which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling [2]. In a given process technology, the maximum supply voltage (referred to as Vmax) for the transistor operation is determined by the process constraints such as gate-oxide reliability limits.Vmax is reducing with the technology scaling due to scaling of gateoxide thickness. The minimum SRAM supply voltage, for a given performance requirement (referred to as Vmin), is limited by the increased process variations (both random and die-to-die) and the increased sensitivity of circuit parameters at lower supply voltage. With the technology scaling, is increasing, and this closes the gap between Vmax and Vmin[5]. Hence, to enable SRAM bit cell operation across a wide voltage range, Vmin has to be further lowered. Various design solutions such as read-write assist techniques and bit cell configurations have been explored. Read-write assist techniques control the magnitude and the duration of different node biases (such as word-lines, bit lines, bit cell VSS node, and bit cell VCC node). In this case, SRAM Vmin can be lowered without adding extra transistors to the six–transistor (6T) bit cell. Various bit cell topologies are also proposed to enable low-voltage operation. In this work, focus will be only on various bit cell configurations. I believe that read-write assist circuits can be applied to these bit cell configurations for further Vmin reduction. Efficient power management is becoming increasingly important with the rapid growth of portable, wireless, and battery-operated applications. Lowering the supply voltage reduces the dynamic power quadratically and leakage power exponentially. Hence, supply voltage scaling has drawn major attention for the low power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor. However, the remarkable decrease in power consumption at ultralow voltage operation is achievable at the cost of processor performance and circuit robustness under process and temperature variation. As the supply voltage is lowered the sensitivity of the circuit electrical parameters to process variation increases. Aggressive scaling of transistor dimensions with each technology generation has resulted in increased integration density and improved device performance. Leakage current increases with the scaling of the device dimensions. Increased integration density along with increased leakage necessities

ultralow-power operation in the present power constrained design environment. The power requirement for the battery-operated devices such as cell phones and media devices is even more stringent. Reducing supply voltage reduces the dynamic power quadratically and leakage power linearly to the first order. Hence, supply voltage scaling has remained the major focus of low power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor [1]. With the scaling of MOSFET dimensions, microscopic variations in number and location of dopant atoms in the region of the device induce increasingly limiting electrical deviations in device characteristics [2]. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations. Interdie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell resulting in asymmetrical characteristics. The combined effect of lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold failure, write-failure and access-time failure [3]. Moreover, it is predicted that embedded cache memories, which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling [4].In a given process technology, the maximum supply voltage for the transistor operation is determined by the process constraints such as gate-oxide reliability limits. Vmax is reducing with the technology scaling due to scaling of gate-oxide thickness. The minimum SRAM supply voltage, for a given performance requirement (Vmin), is limited by increased process variations and the increased sensitivity of circuit parameters at lower supply voltage. With the technology scaling, Vmin is increasing, and this closes the gap between Vmax and Vmin. Hence, to enable SRAM bitcell operation across a wide voltage range, Vmin has to be further lowered. Several design solutions such as readwrite assist techniques and bitcell configurations have been explored [5]. Primary goal of this paper is to reduce the total power dissipation **S**RAM makes up a large portion of a system-on-chip area, and most of the time, it also dominates the overall performance of a system. In addition to this, the tremendous growth in the popularity of mobile devices and other emerging applications, such as implanted medical instruments and wireless body sensing networks, necessitates the requirement of low-power SRAMs. Therefore, a robust low-power SRAM circuit design has drawn great research attention and has become important [1]–[3]. However, a design of robust low-power SRAM faces many process and performancerelated challenges. This is because, in deep submicrometer technology, near/subthreshold operation is very challenging due to increased device variations and reduced design margins. In addition, with each technology node, the share of leakage power in the total power dissipated by a circuit is increasing [4], [5]. Since, most of the time, SRAM cells stay in the standby mode, thus, leakage power is very important. The increasing leakage current along with process variations leads to large spread in read static noise margin (RSNM) and causes read failures at the tail of the distribution [4]. The conventional 6T SRAM cell suffers from read-currentdisturbance-induced SNM degradation with *V*dd scaling. Moreover, due to increased variations at low supply voltages in advanced CMOS processes, caused by global and local process variations, the read stability and the write stability of 6T SRAM cell degrade to unacceptable level. This is further exacerbated by the half-select

disturb and conflicting read/write requirements [6]. To overcome these challenges, different configurations of SRAM cells, such as 7T [7], [8], 8T [9], 9T [10], [11], and 10T [12]–[15] cells, have been proposed. In these circuits, data storing nodes are fully decoupled from read-access path to overcome the conflicting read/write requirements. This approach offers an RSNM that is almost the same as hold SNM (HSNM), therefore, resulting in better read stability. The conventional 8T [9] uses two extra transistors in the read path and one extra bitline (BL) for reading. However, it suffers from leakage introduced in read path, which further increases with scaling. Liu and Kursun [10] proposed a differential 9T bitcell with read-disturb-free operation. It uses the same BLs for both reading and writing; however, doubling the number of transistors connected to BL increases read-access time. Another 9T SRAM cell proposed in [11] and 10T SRAM cells proposed, independently, in [12]–[14] use the modified versions of buffered read path that reduces the leakage of readaccess path, while simultaneously improving RSNM. Chang *et al.* [15] have proposed a read-disturb-free differential 10T bitcell (hereafter called Chang 10T), which is suitable for bitinterleaved architecture. However, it incorporates two seriesconnected transistors in its write path, which degrade the write ability of the bitcell. It needs write-assist circuits, such as wordline (WL) boosting for a successful write operation, and, hence, increases dynamic power of the cell. These bitcells address the read-disturb problem; nevertheless, having crosscoupled inverter pair topology, similar to conventional 6Tcell, offers little immunity to process variations at low supply voltages. For successful SRAM operation under process, voltage, and temperature (PVT) variations, the stability of the cross-coupled inverter is very important [16].

LITERATURE SURVEY:

NVSRAM is one of the advanced NVRAM technology that is fast replacing the Battery-backed SRAMs that need battery free solutions and long term retention at SRAM speeds. For instant on-off operation better non volatile performance is essential [1].Better SRAM performance in terms of leakage power , access time ,robustness is essential [2].The average power dissipiation should be less [3].The 8T SRAM cell as compared to conventional 6T SRAM cell achieved improved read stability, read current and leakage current [4]. Write power i.e. power dissipiation in SRAM should be less [5]. The issue associated with transistor scaling and power management are addressed [8].The operating voltage for cell should be minimum [6]. The inverters are optimized for high noise margin[7] The use of SRAM is expected to increase in future for both portable and high performance microprocessor. SRAM plays a critical role in modern microprocessor system, portable devices like PDA, cellular phones, and portable multimedia devices [1]. To achieve higher speed microprocessor, SRAM based cache memories are commonly used. The trend of scaling of device brings several challenges like power dissipation, sub threshold leakage, reverse diode leakage, and stability [2]. Nowadays research on very low threshold voltage and ultra-thin gate oxide are in progressive stage, due to reduction in the threshold voltage and the gate oxide thickness. The phenomena like intrinsic parameter

fluctuation, random dopant fluctuation, oxides thickness fluctuation, and line edge roughness further degrade the stability of SRAM cells [3-5]. Jaydeep P. Kulkarni [1]. The proposed shows ultra-voltage operation of different SRAM cell is explained The ultra-voltage operation is performed by lowering the supply voltage. The proposed ST-2-bit cell gives 1.6 times higher read static margin and 2 times write static margin as compare to 6T SRAM. For achieving low voltage operation 6T/8T/10T/ST SRAM topologies are studied in this paper. Results are carried out at 130nm technology, which give the effectiveness of proposed bit cell for successive ultra-low voltage operation. Mohsen Imani, Haleh Alimohamadi [2] proposed low power 12T SRAM cell with 16nm at 800mv supply voltage CMOS technology. The proposed 12T SRAM cell is compared with the 9T and 10T SRAM cell which shows that the leakage current is reduced by using two stack transistors at read path. The reliability of cell also increases by increasing read SNM. The proposed cell has 5.5% and 27.4% higher read SNM from 9T and 10T respectively. The power consumption of proposed 12T cell has lowered by 35.5% and 43.8% as comparison of 9T cell and 10T cell. Ambrish Mall, Suryabhan Pratap Singh, Manish Mishra, Geetika Shrivastava[3], states that this paper gives the brief development in low power circuit. In standby mode the power consumption is more. The proposed circuit contains a series connected tail transistor which turn down the leakage current which results in, low power consumption of cell. The proposed 12T SRAM cell is compared with low power 10T SRAM cell on 45nm and 32nm technology, it gives the power reduced by 45.94% (0.4v) and 31.08% (0.3v) respectively. K.G.Dharani [4], this paper gives the comparative analysis of 6T, 8T and 12T SRAM memory cell by power, layout and current values of the cell. In 6T, 8T, 12T the current values may be change during read and write operation but the power consumption is increased in 12T. But 12 T has a high capability to hold the data in the memory. This paper specifies that 6T has very less read margin with 8T transistor however 8T has high write noise margin. Mekala Tajeswar, P. Brundavani[5] ,in this paper, the operation of 12T SRAM cell on multi threshold CMOS technology are studied. This paper gives the reduction in power consumption of SRAM cell by adding transmission gate.By applying two sleep transistors the leakage current during hold mode is reduced and by applying two voltages at the output swing voltage is reduced. On the basis of power consumption, the proposed 12T SRAM cell is compared with the 6T SRAM cell, which shows that the power dissipation in 6T SRAM is 0.182mw and power dissipation at 12T SRAM is 0.169mw. Proposed clearly indicates 12T SRAM gives the better performance and high speed data transmission with or without recovery boosting technique. M.Gangasukanya, P.Asiya Thapaswin[6], this paper introduced a 12T SRAM with high data transmission speed at 45nm technology and low power consumption. In this paper, proposed 12T SRAM cell is studied at different temperature. The proposed SRAM cell has two high voltage sleep transistor and a low Voltage transistor to minimize the power consumption during changing of mode from hold to active mode, so that the static power is also reduced in the cell. By applying two voltages at the output the dynamic power is reduced in this paper. The first voltage is applied to the bit line and second voltage is applied to the bit line bar, which overcomes the swing voltage so that the reduction in swing voltage there in reduction in leakage current also during hold mode this technique the power consumption of

SRAM cell is reduced. P.Pavan Kumar, Dr. R Ramana Reddy, M.LakshPrasanna Rani[7],this paper introduced the 4T SRAM with low power consumption. The proposed 4T SRAM is compared basic structure of 4T SRAM. The software used for this project was mentor graphics at 130nm technology. The NMOS and inverter were used to design the proposed 4T SRAM.

EXISTING TECHNIQUE:

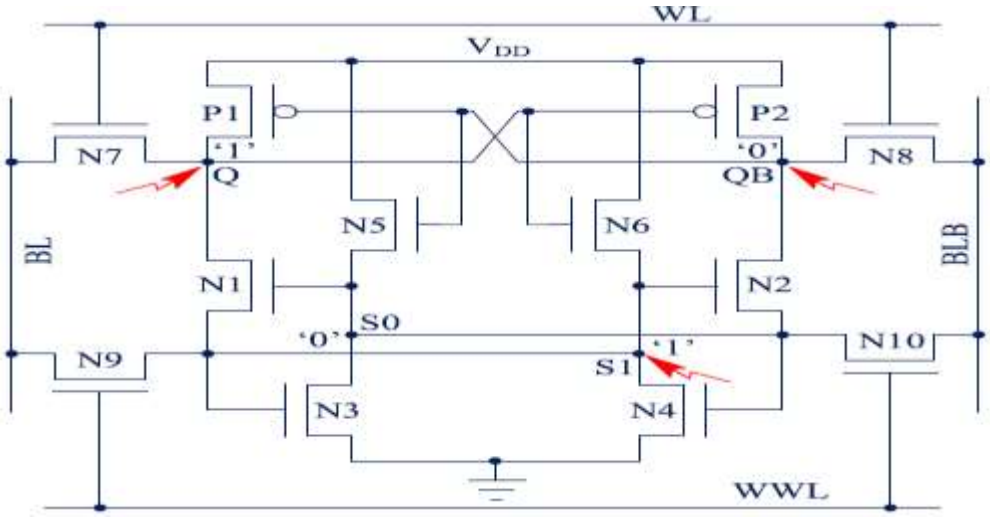

Fig. 1. Schematic of the proposed SARP12T SRAM cell.

we propose the Soft-Error-Aware Read-Stability-Enhanced Low-Power 12T (SARP12T) SRAM cell (Fig. 1) in this paper. SARP12T has the following salient features:

1) SARP12T is immune to SEUs of both polarities induced at any sensitive node.

2) The proposed cell can recover from SEMNUs that occur
at its storage node-pair.

3) SARP12T consumes the lowest hold power among all the considered cells.

4) SARP12T shows enhanced read stability as the '0'-storing storage node, which is directly accessed by the bitline during read operation, can recover from any upset.

5) The proposed cell shows higher write ability and shorter write delay than most of the comparison cells.

EXISTING SARP12T CELL AND ITS OPERATION

The schematic of SARP12T and its equivalent layout are shown in Fig. 1 and Fig. 2, respectively. SARP12T has two wordlines, WL and WWL, two storage nodes, Q and QB, and two internal nodes, S1 and S0. WL controls the access transistors N7 and N8, which connect the storage nodes Q and QB with their corresponding bitlines BL and BLB. The internal nodes S1 and S0 are connected to their corresponding bitlines BL and BLB through their corresponding access transistors N9 and N10, which are controlled by WWL. Let us contemplate SARP12T and all the comparison cells storing '1', i.e., Q = '1' and QB = '0'.

Thus, S1 and S0 are storing '1' and '0', respectively. With this consideration, the basic operations and SEU recovery analysis of SARP12T are explained below.

A. Basic Operations

All the basic operations of the proposed SARP12T are mentioned in this sub-section.

1) Hold Operation: During hold mode, both pairs of access transistors are kept OFF by pulling down both WL and WWL to GND. In order to shorten the read delay, bitlines are kept precharged to *V*DD during hold mode. Therefore, while the cell is in the hold state, transistors P1, N2, N3 and N6 remain ON, while the rest of the transistors remain OFF for the considered case. Thus, SARP12T maintains its initial stored data (Fig. 3).

2) Write Operation: During write operation, both the wordlines (WL and WWL) are activated. Therefore, both pairs of access transistors (N7/N8 and N9/N10) are turned ON. For altering the stored data (i.e., writing '0' at Q), BL is connected to GND, whereas BLB is clamped at *V*DD. As BL is connected to GND, nodes Q and S1 are pulled down by BL through N7 and N9, respectively. Subsequently, node Q turns ON P2 and turns OFF N6, whereas node S1 turns OFF N2 and N3. In the meantime, nodes QB and S0 are pulled up by BLB through N8 and N10, respectively. Consequently, node QB turns OFF P1 and turns ON N5. Similarly, node S0 turns ON N1 and N4. The cross-coupling between P1 and P2 amplifies the potential difference between Q and QB. Similarly, the cross-coupling between N3 and N4 enhances the potential difference between S1 and S0. Therefore, the write operation is performed successfully (Fig. 3).

3) Read Operation: During read operation, WL is connected to *V*DD, whereas WWL is kept deactivated. Therefore, access transistors N7 and N8 are turned ON, while the other access transistors (N9 and N10) remain OFF. For read operation, bitlines are precharged to *V*DD. Therefore, BLB discharges through N8, N2 and N3. On the other hand, as N1 and N4 are OFF, BL stays at *V*DD (Fig. 3). Once the voltage difference between BL and BLB reaches 50 mV, a sense amplifier (not shown) can sense the stored data, which completes the read operation.

B. SEU Recovery Analysis

This sub-section gives a brief discussion of the proposed cell when its sensitive nodes are affected by an SEU. A sensitive node is the surroundings of the reverse biased drain diffusion region of an OFF transistor. If a radiation particle strikes the drain terminal of a PMOS, it produces either a '0'_'1' or '1'_'1' transient pulse, based on the data that the node was storing initially. On the other hand, if an energetic particle strikes an NMOS, it generates either a '0'_'0' or '1'_'0' transient pulse. It is to be noted that, as the '0'-storing internal node (S0) of SARP12T is surrounded by drain terminals of only NMOS transistors, only a '0'_'0' spike is generated, which does not affect the logic state of the node. Hence, for the '1'-storing case of SARP12T (i.e, Q = '1', QB = '0', S1 = '1' and S0 = '0'), node S0 is not sensitive, whereas the other nodes, i.e., Q, QB and S1, are sensitive. *1) SEU @ S1:* When the '1'-storing internal node S1 is affected by an SEU, the node value changes from '1' to '0' (Fig. 3). Consequently, transistors N2 and N3 are turned OFF. However, the pull-up transistor P2, corresponding to QB, is kept OFF by the unaffected node Q. Since, both

the pull-up and pull-down paths corresponding to QB are disconnected, node QB goes to a high impedance state. Generally, a high impedance state does not change the logic state of the node. Hence, QB maintains its initial logic value and keeps N5 OFF. Therefore, S0 also goes to a high impedance state (as N5 and N3 are OFF) and retains its initial logic value. Since Q, QB and S0 retain their states, S1 recovers its original state (Fig. 3). *2) SEU @ Q:* When '1'-storing storage node Q is influenced by an SEU, the logic state of the node transits to '0' (Fig. 3). Therefore, transistors P2 and N6 are temporarily

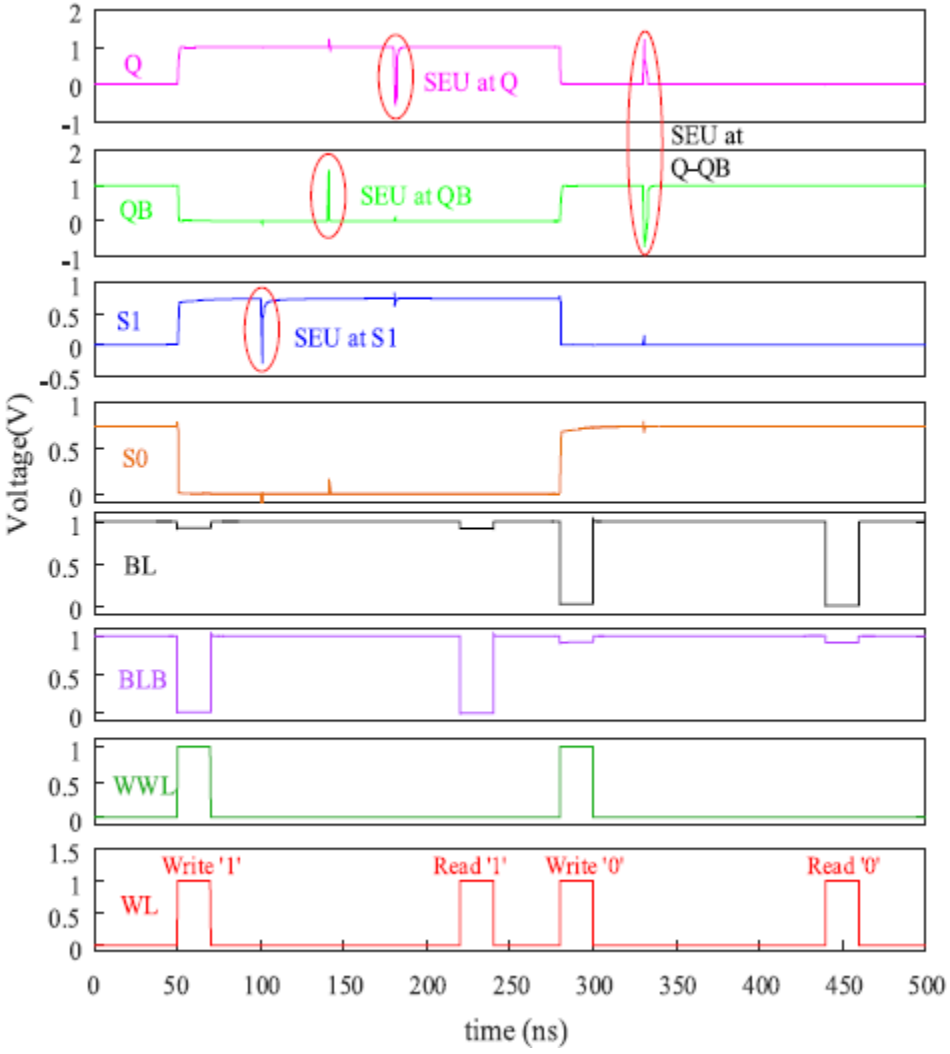

Fig. 3. Sequence diagram of basic operations and soft-error recovery at

different nodes of the proposed cell. turned ON and OFF, respectively. Since N6 is turned OFF and N4 remains OFF (by virtue of its hold mode), node S1 goes to a high impedance state and retains its logic value. Therefore, N2 and N3 remain ON. Though P2 is turned ON, as NMOS transistors N2 (2.5×) and N3 (2.5×) aremade larger than the PMOS transistor P2 (1×), QB stays at its original logic level. Since QB retains its state, P1 remains ON and N5 remains OFF. Furthermore, as N3 is ON, S0 stays at '0' and keeps N1 OFF. Therefore, Q recovers its original data (Fig. 3). *3) SEU@ QB:* When an SEU of enough strength influences '0'-storing storage node QB, the logic value changes to '1' (Fig. 3). Subsequently, P1 is temporarily turned

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OFF and N5 is temporarily turned ON. Though N5 is turned ON, node S0 retains its logic state because N3 (remains ON by virtue of itshold mode) is made larger (2.5×) than N5. Therefore, N1 and N4 remain OFF. Since both the pull-up (P1) and pull down (N1) transistors corresponding to Q are OFF, node Q goes to a high impedance state and retains its initial logic state. As N4 remains OFF and N6 (driven by Q) remains ON, S1 stays at its original logic value and keeps N2 and N3 ON. Hence, nodeQB is discharged to GND (Fig. 3).

4) SEMNU @ Q-QB: When both the storage nodes Q and QB are simultaneously affected due to an SEMNU, node Q transits from '1'_'0' and node QB changes from '0'_'1'. Therefore, Q turns ON P2 and turns OFF N6. Similarly, QB turns OFF P1 and turns ON N5. Though N5 is turned ON, node S0 retains its logic level (as explained in Section II-B.3). Since the logic state of S0 is unaffected, transistors N1 and N4 remain OFF. As both N6 and N4 are OFF, node S1 goes to a high impedance state and stays at its original logic state. Therefore, N2 and N3 remain ON, and hence, QB is discharged to GND. Since N1 is OFF (as S0 retains its state) and P1 is turned ON (as driven by QB), node Q is brought back to '1'. Therefore, both Q and QB recover their original states. Therefore, the proposed SARP12T cell can recover from the effect of an SEU induced at node S1 or Q or QB, and can also recover from an SEMNU induced at the Q-QB node-pair. However, if enough charge is collected at the node-pair S1-Q/S1-QB, node S1 may transit from '1'_'0', which turns OFF N2 and N3, whereas node Q/QB may alter from '1'_'0'/'0'_'1', which turns OFF N6/P1 and turns ON P2/N5.

PROPOSED TEHNIQUE:

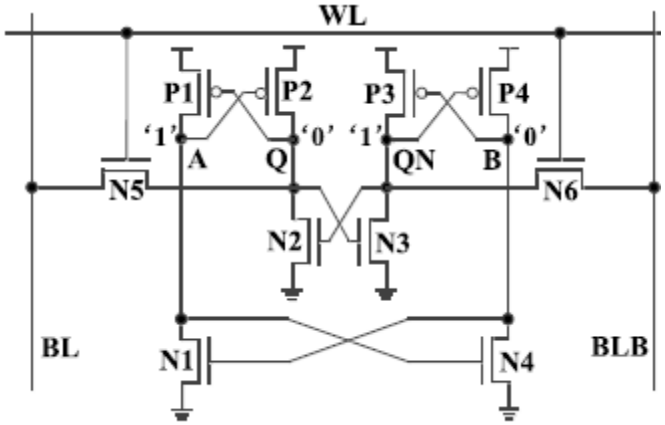

Fig. 2. Proposed quadruple cross-coupled storage cell QUCCE 10T.

The QUCCE 10T is proposed for highly reliable high-density terrestrial applications at the nominal supply voltage. The QUCCE 12T is a promising candidate for future highly reliable terrestrial low-voltage applications.

Cell Structure and Behavior

The QUCCE 10T memory cell has four storage nodes A, Q, QN and B. The output nodes, Q and QN, are connected to the bit lines BL and BLB through pass gates N5 and N6 respectively. The two access transistors N5 and N6 are controlled by word line WL and will be enabled when WL is at high logic state. The stored '0' state for the proposed QUCCE 10T cell is taken into consideration. As is shown in Fig. 2, the logic states of nodes A, Q, QN and B are '1', '0', '1' and '0' respectively.

1) In hold mode, as is depicted in Fig. 4, the logic state of word line (WL) is set to be '0' and thus the two pass gates N5 and N6 are disabled. Each of the four nodes is determined by an NMOS transistor and a PMOS transistor in series. Transistors P1, N2, P3 and N4 are turned on while transistors N1, P2, N3 and P4 are turned off.

2) For read operation, two bit-lines BL and BLB will be pre-charged to supply voltage in a first step and WL is set to be '1' state to activate access transistors N5 and N6 afterwards. As for the 'read 0' operation in Fig. 4, BLB will maintain its original states without being changed, but BL will be discharged because N5 and N2 are turned on, creating a path from BL to ground. The voltage difference obtained from BL and BLB will be amplified by a differential sense amplifier and output the data stored in the memory cell. In order to obtain stable read operation, CR, the cell ratio defined as (WN2/LN2)/(WN5/LN5) or (WN3/LN3)/(WN6/LN6), should be set properly to acquire good RSNM and ensure integrated density at the same time.

3) To change the original stored data of the QUCCE 10T cell in Fig. 2, WL and BL are set to be '1' while BLB is set to be '0' to carry out the 'write 1' operation shown in Fig. 4. Once the access transistors N5 and N6 are activated, BLB pulls down the potential at node QN through transistor N6 below the threshold voltage (VTH) of transistor N2 resulting in N2 being turned off, and BL pulls up the potential at node Q through transistor N5 towards (VDD-VTHn). Meanwhile, the crosscoupled latch structure composed of transistor N2 and N3 will further amplify the voltage difference between node Q and QN, accelerating the buildup of voltage difference. Notice that N6 has to be stronger than P3 to realize this. The related pull-up ratio, PR1, is defined as (WP2/LP2)/(WN5/LN5) or (WP3/LP3)/(WN6/LN6). Furthermore, another cross-coupled latch structure composed of transistor P3 and P4 will amplifier the voltage difference between node QN and B. In order to pull up the potential at node B, P4 has to be stronger than N4. The related pull-up ratio, PR2, is defined as (WP4/LP4)/(WN4/LN4) or (WP1/LP1)/(WN1/LN1). Considering PMOS transistor has smaller carrier mobility than NMOS transistor, to get a stronger P4 or P1 will cost more area overhead. In a successful write operation, nodes Q and QN will eventually be modified to new data. Transistors N1, P2, N3, and P4 are turned on, and transistors P1, N2, P3, and N4 are turned off. Nodes A, Q, QN and B are set to be '0', '1', '0' and '1' respectively.

B. SEU Recovery Analysis

Taking the state shown in Fig. 2 into consideration, nodes A, Q, QN and B are sensitive nodes and they are set to be '1', '0', '1' and '0' respectively.

1) If node A is affected by an SEU, node A will be discharged to 0 logic state and its original logic high state will be upset. In this case, transistor N4 will be turned off and transistor P2 will be turned on. Since transistor P2 is turned on, both transistor P2 and N2 will be activated and they will compete with each other making node Q unstable. Meanwhile, transistor N4 turned off, node B will be at high impedance state and its value will be kept. In normal condition, the high impedance state will not influence the logic state of the related node. Therefore, only node A and node Q will be affected, and node QN and node B will still keep their right value. Node Q will get steady and recover as a result of the persistent correct signal from node QN, and it will further correctly bias the transistor P1 making node A regain its original logic high state. Due to the symmetric structure of the QUCCE 10T cell, analyses are similar to that of the node QN.

2) If node Q is affected by a particle-induced glitch, node Q will be charged to logic high state. In this case, transistor N3 will be turned on and transistor P1 will be turned off. Since transistor N3 is activated, node QN will be unstable. Transistor P1 turned off, node A will be at high impedance state and its value will be kept. Nodes A and B maintain their logic state. Thus node QN and node Q will recover from node B and restored node QN, respectively. However, if the particle-induced charge collected at node Q is sufficiently large, the unstable node QN will be upset and the cell still can be flipped. Analyses are similar to that of the node B.

QUCCE 12T SRAM BIT-CELL

A. Cell Structure and Behavior

The QUCCE 12T memory cell has four storage nodes A, Q, QN and B. Node Q and B are connected to BL through access transistor N5 and N7 respectively while node QN and A are connected to BLB through access transistor N6 and

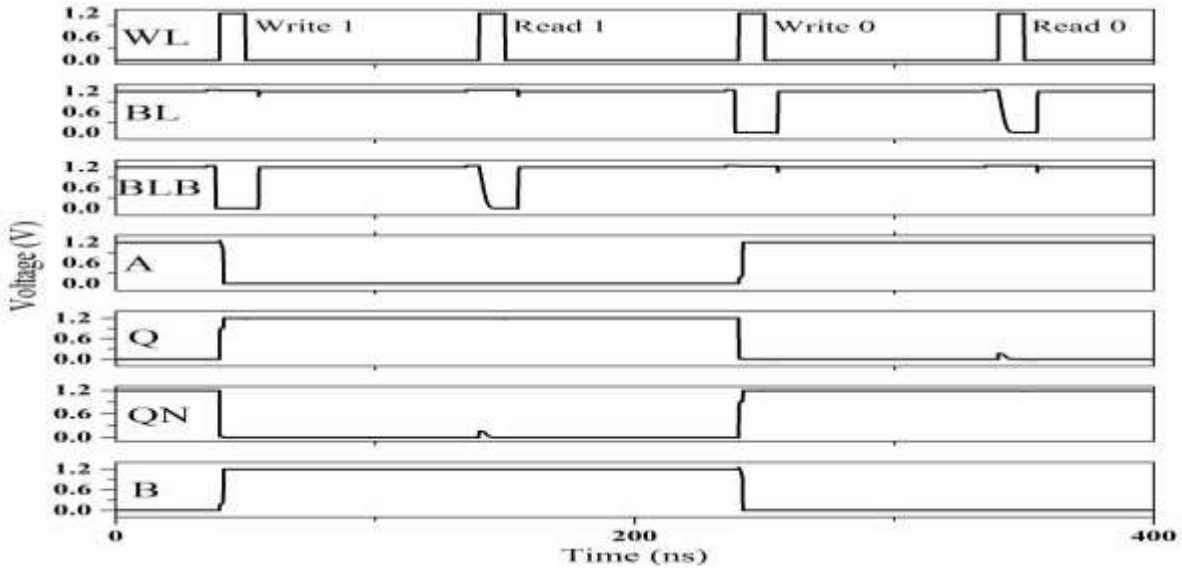

Fig. 4. Simulation of whole functional operations of QUCCE 10T.

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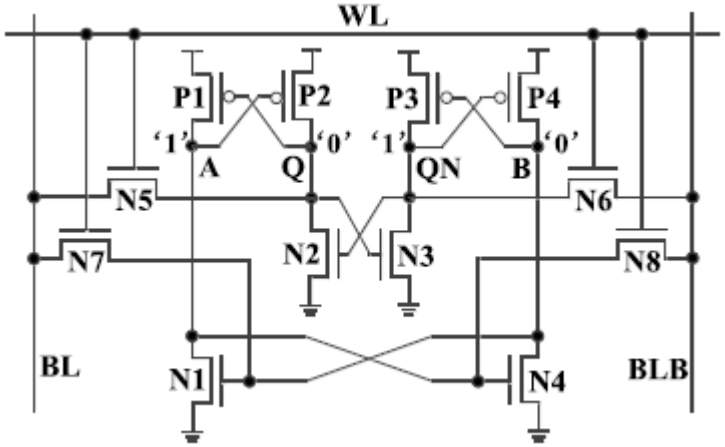

Fig. 5. Proposed quadruple cross-coupled storage cell QUCCE 12T.

N8 respectively. Access transistors N5, N6, N7 and N8 are controlled by word line WL and will be activated when WL is set to be high. As is presented in Fig. 5, the stored '0' value is assumed and the four storage nodes A, Q, QN and B are set to be '1', '0', '1' and '0' respectively. 1) In hold mode, as is presented in Fig. 7, WL is discharged to '0' state to turn off the four pass gates N5, N6, N7 and N8. Transistors P1, N2, P3 and N4 are turned on while transistors N1, P2, N3 and P4 are turned off. Thus storage nodes A, Q, QN and B keep their original value without being changed. 2) For read operation, two bit-lines BL and BLB will be pre-charged to supply voltage and afterwards WL will be charged to VDD to turn on pass gates N5, N6, N7 and N8. As for the 'read 0' operation in Fig. 7, BLB will keep its original state because it connects to two logic high state nodes QN and A through transistors N6 and N8 respectively. Meanwhile, BL will be discharged through two paths, one from transistor N5 and N2 to the ground, and the other from transistor N7 and N4 to the ground. The voltage difference obtained from BL and BLB will be rapidly amplified by a differential sense amplifier and afterwards the data stored in the memory cell will be output. Due to the two discharging paths, the QUCCE 12T cell acquires a high speed read operation since the necessary voltage difference is much easier got than memory cells possessing a single discharging path. To obtain stable read operation, CR, the cell ratio defined as (WN2/LN2)/(WN5/LN5), (WN4/LN4)/(WN7/LN7), (WN3/LN3)/(WN6/LN6), or (WN1/LN1)/(WN8/LN8), should be set properly to acquire good RSNM and ensure integrated density at the same time. 3) In order to write '1' into the QUCCE 12T cell, as Fig. 7 portrays, WL and BL are set to be '1' while BLB is set to be '0'. The access transistors N6 and N8 activated, BLB pulls down the potential at nodes QN and A to be '0' and thus transistors N2 and N4 are turned off while transistors P2 and P4 are turned on, resulting in nodes Q and B being charged to be '1'. On the other side, the access transistors N5 and N7 enabled, BL pulls up the potential at node Q and B through transistor N5 and N7 towards (VDD-VTHn) respectively. The pull-up strength of high state bit-line is weak because of an NMOS threshold voltage (VTHn) drop. Meanwhile, the cross-coupled latch structures will further amplify the voltage difference between the related node pairs in the latch, accelerating the

buildup of voltage difference. In this case, transistors N1, P2, N3 and P4 are turned on, and transistors P1, N2, P3 and N4 are turned off. Nodes A, Q, QN and B are changed to be '0', '1', '0' and '1' respectively. Unlike QUCCE 10T cell, QUCCE 12T cell only has one pull-up ratio PR defined as (WP3/LP3)/(WN6/LN6), (WP1/LP1)/(WN8/LN8), (WP2/LP2)/(WN5/LN5), or (WP4/LP4)/(WN7/LN7).

B. SEU Recovery Analysis:

Taking the state shown in Fig. 5 into consideration, storage nodes A, Q, QN and B are sensitive nodes and they are set to be '1', '0', '1' and '0' respectively. Any sensitive node being affected by SEU, recovery analyses are similar to that of the QUCCE 10T.

C. Implementation

The proposed QUCCE 12T memory cell, the nominal supply voltage of which is 1.2 V, has been implemented in 130 nm CMOS technology of HHGrace. The layout of the cell in Fig. 6 has been accomplished in the Cadence Virtuoso. CR, the cell ratio defined as (WN2/LN2)/(WN5/LN5), (WN4/LN4)/(WN7/LN7), (WN3/LN3)/(WN6/LN6), or (WN1/ LN1)/(WN8/LN8) for read stability, is set to be 1.8. PR, defined as (WP3/LP3)/(WN6/LN6), (WP1/LP1)/(WN8/LN8), (WP2/LP2)/(WN5/LN5), or (WP4/LP4)/(WN7/LN7) for writeability, is set to be 1. Simulations were performed with HSPICE to show the whole functional operations of the proposed QUCCE 12T cell. In Fig. 7, 'write 1', 'read 1', 'write 0' and 'read 0' operations are simulated to verify the whole functional operations of the proposed QUCCE 12T cell.

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RESULTS:

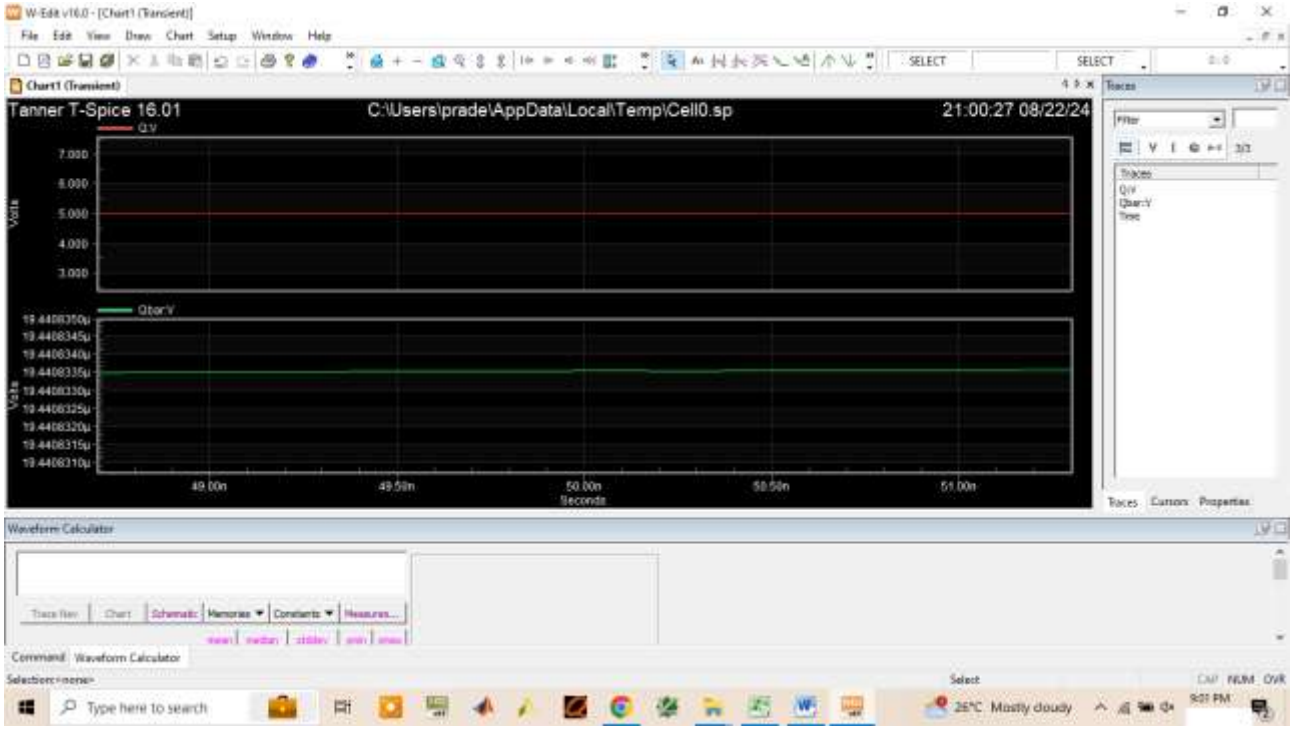

Table: Comparison table

PARAMMETER	PROPOSED	EXISTING
POWER (W)	1.121e-15	2.167e-13
TIME (S)	0.70	1.36

CONCLUSION:

In this paper, a soft-error-aware read-stability-enhanced low power SRAM cell is proposed for aerospace applications. SARP12T can regain its original data at all the sensitive nodes, even if the node values are flipped by a radiation strike. Furthermore, SARP12T can recover from the effect of multi-node upset due to a single ion strike at the storage node-pair. In addition to these advantages, the proposed cell also exhibits the highest RSNM and consumes the lowest hold power, while also showing better write performance compared to most of the comparison cells. Moreover, SARP12T proves its superiority over other contemporary cells by exhibiting the highest EQM. Therefore, the proposed SARP12T can be considered a better choice for aerospace applications.

FUTURE SCOPE: CLOCK RATE AND POWER can be reduced by using modified architectures as follows. The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have nearly negligible power consumption when sitting idle, in the region of a few micro-watts.

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