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Multilevel inverter technology for enhanced ev performance

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ABSTRACT: -Multilevel inverters' (MLI) effective and small design is motivating for a variety of applications, including solar photovoltaics (PV) and electric vehicles (EV). A 53-Level multilevel inverter topology based on a switched capacitor (SC) technique is proposed in this paper. The amount of SC cells and their cascade link determine how many MLI levels are needed. The output voltage can be implemented at levels 17 and 33 by cascading the SC cells. For the higher levels, the suggested structure is simple to use and implement. There are fewer driving circuits when there are fewer active switches. As a result, the MLI's device count, price, and size are all decreased. A perturb and observe (P&O) algorithm and the solar panels work together to provide a steady DC voltage that is boosted over the DC link voltage using a single input and multi-output converter (SIMO). Experimental testing is done on the suggested inverters with rapid load disturbances and dynamic load changes. This depicts an electric car travelling on several types of roads. A thorough comparison is done in terms of

the quantity of switches, gate driver boards, sources, diodes, and capacitors, and factor for component count. The simulation findings for the 17-level, 33-level, and 53-level MLI are validated using total harmonic distortion (THD) is found to be the same and less than the experimental results. 5%, in accordance with IEEE guidelines. While MATLAB/Simulink is used for the simulations, a hardware prototype is developed in the laboratory and confirmed experimentally under dynamic load fluctuations.

INDEX TERMS: - Photovoltaic (PV) system, multilevel inverter, electric vehicles (EVs), maximum power point tracking (MPPT), and total harmonic distortion (THD).

I. INTRODUCTION

As the need for high-quality power quality in industrial applications and solar photovoltaic systems grows, the desired parameters, such as a clean sine-wave output and fewer harmonic distortions, are met by traditional inverters is a difficult undertaking. More is given to the multilayer inverters, focus on fulfilling the necessary conditions and serves as a substitute for providing a certain level of power. It offers various benefits, including fewer devices, function in reduced harmonic distortions, less dv/dt stress, low switching frequency, etc. [1]. Recent multilevel inverter topologies, like the flying capacitor type (FC) [2], cascaded H-bridge type (CHB) [3], and neutral point clamped type (NPC) [4], use fewer circuit components than ordinary inverters. Cost and complexity are increased by the direct proportionality between the number of components in the circuit and the number of levels in MLI [5]. The capacitor voltage balancing in the FC MLI and NPC MLI is a difficult process that is restricted to five levels and is not capable of cascading.

As a result, there are greater losses and a high switching frequency with half the input voltage [6]. Many topologies are suggested based on the different levels that are facing their own issues, and a wide variety of study is lowering the components of MLI [7], [8].

Different MLI topologies that are unrelated to the traditional three categorization classes have been published in [9]–[13] in the recent past. Importantly, [15] proposes sub multilevel converter configurations. A basic level topology that requires numerous dc voltages is detailed in [10]. The topologies based on coupled inductors are documented in references [9] and [11]. Although these structures are straightforward, it can be difficult to expand them to higher levels. The output voltage levels of the novel MLI topologies, which are based on switched-capacitor (SC) with boost techniques, are limited to 5, 7, and 13, respectively, in [12] and [13]. It is possible to extend the MLI topology suggested in [14] to higher levels. The cost and size of the system rise with the use of multiple switches and devices.

About the switched capacitor (SC) method, [16] presents a new MLI topology featuring a full bridge and a multilayer converter. Two diodes make comprise a five-level single phase inverter with a full bridge. In [17], a single switch is shown with five levels in its output and circuitry that restricts the extension of higher levels. A frontend SC is made up of the SC-based MLI topology described in [18], and the application is limited by the control complexity, additional devices, and a full-bridge backend. A high switching loss

makes it impossible to resist producing a high-frequency output because the carrier frequency supplies the switching frequency [51]. Theoretically, a boost MLI with a partial charging SC method can increase the number of output voltage levels. Partial charging implementation involves a significant level of control complexity [12]. Therefore, creating a high-frequency output, low harmonic content, and highly efficient SC-based MLI is a difficult task [19]. Due to the system's reduced weight and compactness, the high-frequency output is appropriate for incorporating circuits in electric vehicles (EVs) [20].

Solar PV panels make up the photovoltaic power generation system. A DC-DC converter is used to feed the solar panel's output to the DC link. The DC-AC inverter and load receive voltage via a DC link [21]. Temperature and solar radiation have an impact on the output of photovoltaic systems, which is not constant [22]. To ensure that photovoltaic panels operate efficiently in the face of varying climate conditions, it is imperative to maximise the power output of the module, a process known as maximum power point tracking, or MPPT [23]. A DC-DC converter, which operates with the duty cycle change, is crucial to managing maximum power whenever the MPPT is present in a system [24].

A control method is required for a PV supplied inverter to produce a steady DC voltage. A typical PI controller implemented in the independent photovoltaic system to choose a appropriate DC-DC converter duty cycle by contrasting the output of the converter with citation [25]. Having is not something that is desirable using the MPPT approach to get control over the DC-DC converter, and hence several topologies are suggested to address this problem, regarding the independent solar power system. Several cutting-edge methods, including artificial intelligence (AI), fuzzy logic, genetic algorithms (GA), and practical swarm optimisation (PSO), have been developed recently to have an auto-control regarding the training data to regulate voltage [26]. It is an incredible work to choose the MPPT methodology for a certain application, as each method has pros and cons of its own. The MPPT methods, such as hill climbing (HC), perturbation, and observation (P&O), are commonly employed due to their straightforwardimplementation. Conventional techniques such as fuzzy, P&O, and INC algorithms are unable to extract global MPP (GMPP) under partial shade situations [27].

Several literary works have used MLI with DC connection with MPPT, allowing for output control by the load [28] or under constant solar irradiance [29]. Depending on the load, temperature, and solar irradiation, MPPT continuously modifies the solar panel's energy to run at its maximum power. Temperature and sun irradiation vary throughout the day based on the weather and the time of year. Thus, keeping an eye on each of these factors is essential to achieving optimum PowerPoint.

This study presents the implementation of a solar PV system with a 53-level multilevel inverter integrated with a single input and multiple output DC-DC boost converter. The suggested system uses the P&O powered MPPT technology to maximise the energy produced by the solar panels. DC electricity from the solar panels is fed to a single input, multiple

Industrial Engineering Journal
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output boost converter, which raises the voltage to the required level before feeding it to a 53-level inverter. The output voltages of 17, 33, and 17 levels are obtained by cascading the SC units. The performance of these MLIs is compared with different MLI topologies and is represented based on numerous characteristics such as device count, power losses, efficiency, and THD. MATLAB/Simulink is used to test the implemented system, while its setup.

The study is structured as follows: PV Modelling and one input and several outputs A DC-DC boost converter is the suggested 53-level MLI modelling using the SC units cascade combinations to provide 17 and 33-level MLIs, along with the power loss calculations, are displayed in section II in the third segment. The outcomes of the experiment and simulation are outlined in Section IV. Multiple analogies using the same and different MLI topology levels are shown in section V. Section VI concludes with some final thoughts.

II. MODELLING OF PV AND DC-DC BOOST CONVERTER

A. MODELLING OF SOLAR PV

An essential part of the analysis of a solar PV system is the modelling of a solar cell. The entire suggested circuit consists of solar panels and the 53-level MLI seen in Figure 1 as well as a three-level DC-DC boost converter. Three categories can be used to simulate solar photovoltaics: an equivalent circuit with current-voltage (I-V) and power-voltage (P-V) characteristics; the impact of temperature and sun irradiation; and

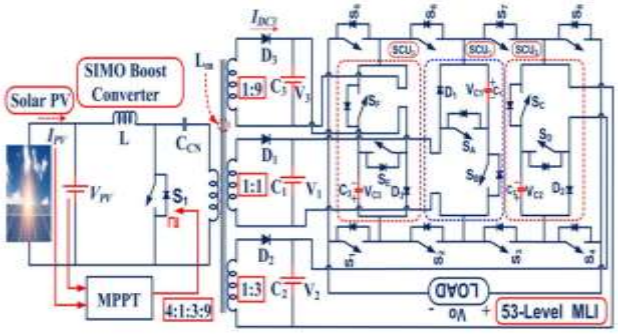

FIGURE 1. Overall structure of the proposed system.

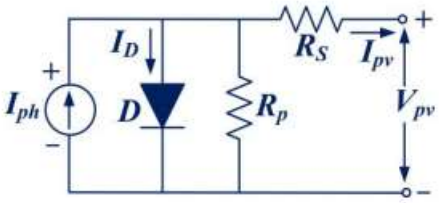

FIGURE 2. Equivalent circuit of solar cell.

The circumstance of partial shadowing is considered. PV is a compound word that combines the words photo and voltaic: photo is used to represent photonic energy, and voltaic is used to represent electrical energy. This suggests that photonic energy can be converted into electrical energy [30]. A solar array is made up of different kinds of modules, each of which has solar cells in it. P-n semiconductor diodes are included in this [31]. The intended solar PV system exhibits a behaviour whereby its output varies in response to variations in temperature and meteorological variables [32]. As a result, the following represents the factors in modelling a solar PV system:

1)SOLAR CELL: EQUIVALENT CIRCUIT AND I–V CHARACTERISTICS

The solar cell is made up of internal resistances RSE and RSH that are connected in series and parallel to the

Industrial Engineering Journal
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Volume : 53, Issue 11, November : 2024

diode; FIGURE 2 illustrates this analogous circuit. The output voltage and current of a solar cell are denoted as VPV and IPV, respectively. These come from connecting many PV modules in series and parallel, as indicated by equation (1).

$$I_{PV} = \left\{ I_{Ph} - I_0 \left[exp\left(\frac{q(V_{PV} + R_{SE} I_{PV})}{N_{SE} AKT} \right) - 1 \right] - \frac{(V_{PV} + R_{SE} I_{PV})}{N_{SE} R_{SH}} \right\} \quad (1)$$

where NSE and NSH represent the number of PV cells connected in parallel and series, respectively. The parallel resistance is denoted by RH, and the series resistance by RSE. A semiconductor device's idealist factor is denoted by A. T is the temperature, while K is Boltzmann's constant (1.3806503 × 10−23 J/K). The produced current, or IP, is dependent on the irradiation and temperature shown in equation (2)

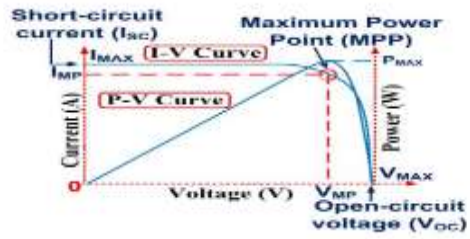

FIGURE 3. I-V Characteristics of solar cell.

$$I_P = [I_{SK-STM} + K_i (T - T_{STM})] - \left(\frac{G}{G_{STM}} \right) \quad (2)$$

where G (W/m2) is the ground state, Ki is the SCC coefficient, and ISK−STM is the short-circuited current at standard testing cases (STM), the cell's surface irradiance, GSTM (1000W/m2) is the cell temperature is TSTM and the irradiance is at STM [33].

$$I_O = \left\{ \frac{I_{SK-STM} + K_i (T - T_{STM})}{exp\left[(V_{OK-STM} + K_{OV} (T - T_{SKC}) / AV_{Sth} \right]} \right\} \quad (3)$$

where VSth is the solar cell thermal voltage, KOV stands for the open-circuit voltage coefficient, and VOK−STM is the open-circuited voltage at the standard testing case.

$$P_{PV} = V_{PV} \times N_{SH} \left(I_{Ph} - I_O exp\left(\frac{qV_{PV}}{N_{SE} AKT} \right) - \left(\frac{V_{PV}}{N_{SE}} \right) \right) \quad (4)$$

The I-V/P-V curves, which illustrate a solar cell's properties, are displayed in FIGURE 3 [4]. The operating point of a PV exhibits instability, as evidenced by the curve, which continuously swings from null to open-circuit voltage. To designing solar PV at different irradiances, there is a single point in this process that generates peak power. As seen in Figure 3, the corresponding voltages and currents are VMPP and IMPP.

The temperature, quantity of series and parallel connected strings, irradiance, and temperature all affect the current and voltage obtained from solar PV. Thus, it is necessary to select the solar panel carefully. This paper selects the 1Soltech 1STH-215-P panel with two series and parallel connected modules per string from a list of solar module data provided in MATLAB. Table 1 lists the characteristics of the chosen solar panel and provides measurements for one parallel string and one series-connected module at a temperature of 250 °C and 1000 W/m2 of solar radiation.

2) IRRADIANCE AND TEMPERATURE EFFECT

With variations in climate variables, the solar PV production fluctuates continuously [34]. Because the solar irradiance depends on the sun's incidence angle, this effect modifies the I-V/P-V properties. In addition to shifting its magnitude, VPV also causes the output

Industrial Engineering Journal
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Volume : 53, Issue 11, November : 2024

current IPV to vary in tandem with variations in sunray incidence, resulting in a continuous VPV [34]. A solar PV's temperature change is influenced by three factors: When the photovoltaic system was operating, the heat dispersed naturally because the sunbeam intensity gradually increased and the infrared wavelength began to wear on the cell [26]. Based on equations (5) and (6), the VOC and ISC are calculated at varying irradiance.

$$V_{OC} = V'_{OC} + a_2\left(T - T'\right) - \left(I_{SC} - I'_{SC}\right)R_{SE} \quad (5)$$

$$I_{SC} = I'_{SC}\left(\frac{G}{G'}\right) + a_1\left(T - T'\right) \quad (6)$$

The temperature coefficients of the PV cell are a1 and a2, respectively, based on the equations [35]. The reference parameters at solar intensity G' and temperature T0 are V'OC and I'OC.

The output voltage and currents are impacted by specific fluctuations in the climate. The maximum amount of power can be extracted from solar PV at any time during operation. An effective MPPT method that maintains a steady voltage at the output while monitoring temperature and radiation can make this feasible.

3) PARTIAL SHADING EFFECT

In addition to temperature and irradiance, a partial shadowing scenario presents another difficulty for the MPPT technique when trying to maximise power. Mists, buildings that come after one another, trees, etc., all provide this partial shadow [36]. Low illumination results in a decrease in the photocurrent Iph, as stated in equation (2). All the cells in a PV module that is connected in series have the same current. However, in this instance, the photocurrent weakens and the shaded cell undergoes a breakdown, acting as a load rather than a source of energy.

B. MPPT CONTROLLER

An MPPT controller is used in solar PV operation to extract the maximum power from the PV module. The efficiency and lifespan of the solar PV increase if the controller can function well in tracking and supplying peak power from the panels during all the above-mentioned disturbances. This can be accomplished by producing the highest amount of power possible for different climate circumstances by sinking the solar source to the load. There are two methods for getting the most energy out of a solar panel. Both mechanical and electrical tracking are involved. When solar panels are mechanically tracked, their direction changes in response to patterns of climate variation.

TABLE 1. Specifications of the 215W PV system.

Maximum power	213.15W
The voltage at maximum power point (V_{MPP})	29V
Open circuit voltage (V_{oc})	36.3V
Current at maximum power point (I_{MPP})	7.35A
Short circuit current (I_{sc})	7.84A
Diode ideality factor	0.98117
Diode saturation current (I_O)	2.9259×10^{-10}A

This encompasses several months of seasonal variations in the climate. The I-V curve is compelled by electrical tracking to find the PV array's operating point of maximum power [37]. An integral component of the system that supplies the maximum power to the load

Industrial Engineering Journal
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Volume : 53, Issue 11, November : 2024

(batteries/motors) is called the MPPT controller.

An appropriate method must be employed to track the PV module's maximum power usage while it is operating. The P-V graph of a solar cell illustrates this. Numerous techniques exist for tracking the maximum power, including evolutionary algorithms, incremental conductance, perturb and observe, fractional open-circuit voltage, and more. The perturb and observe approach offers numerous benefits in this study. Using different controllers, such Arduino, Microcontroller, etc., makes it simple to implement. The perturbation value can be adjusted to influence the maximum power point determination speed. In Figure 4, the P&O algorithm is displayed.

The following is the algorithm used for the Perturb and Observe Technique:

a) PV module Ipv and Vpv values are obtained.

b) Ppv is computed using Vpv and Ipv.

c) Power and voltage readings are saved.

d) Step "a" is repeated, and the values are recorded for the subsequent (k + 1) th instant.

e) The numbers obtained at the (k + 1) th instant are deducted from the values obtained at the kth moment.

f) The PV curve of a solar panel exhibits a negative slope on the right side (dP/dV<0), while the left side displays a positive slope (dP/dV>0). As a result, the curve's right side corresponds to the lower duty cycle and its left side to the high duty cycle.

g) According to the polarity of slope after subtraction, the algorithm decides the change in the duty cycle.

The solar panel has a 215W design power; the TABLE 1 displays the relevant parameters and their specifications.

C. DC-DC BOOST CONVERTER

Figure 1 [38] depicts a single input multiple output DC-DC boost converter interfaced between the solar panels and the suggested inverter. Three separate DC sources are offered by this converter in the 4:1:3:9 ratio. To remove uneven voltages and step size fluctuations caused by various climatic conditions, the converter runs on a single solar PV.

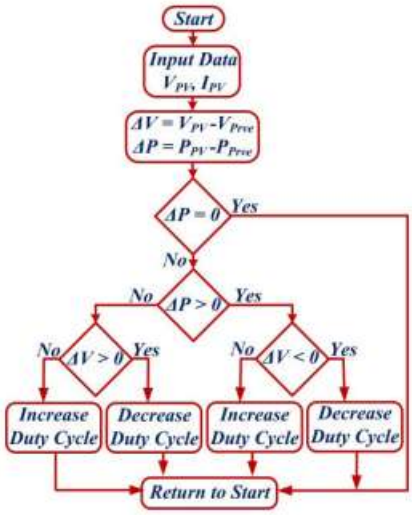


FIGURE 4. Flowchart of P&O algorithm.

The following relation can be used to compute the inductance's magnitude:

$$L = \left(\frac{mV_{dc}}{4af_sI_r}\right) \quad (7)$$

where fs is the switching frequency, Ir is the ripple current, Vdc is the input dc voltage, m is the modulation index, and an is the overloading factor, which is typically 1.25.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

The following relationship can be used to compute capacitance value:

$$C = \left(\frac{DI_{dc}}{V_{dc} r f_s \times 0.5} \right) \quad (8)$$

where D is the duty cycle, Vdc is the input dc voltage, r is the ripple voltage, fs is the switching frequency, and Idc is the dc current.

The following relationship can be used to determine the converter's duty cycle:

$$D = \left(\frac{V_O}{V_O + V_{dc}} \right) \quad (9)$$

Figures 5 and 6 display the findings of the simulation and experiment, respectively. Table II displays the parameters of the boost converter.

III. PROPOSED ASYMMETRICAL 53-LEVEL MLI

A switched capacitor technique is used in the design and implementation of the proposed 53-level MLI. The H-bridge and SC are integrated at the front end. It serves as the projected MLI's separate energy storage system. Therefore, it is crucial to choose the precise capacitance value, which is determined by the operating frequency, the amount of load current needed, and the upper bounds of the added ripple voltage. The advantage of SC's structural design is that it can raise the voltage level. A DC-DC converter must provide a rated output to the inverter; however, with the suggested architecture, voltage is increased based on the charging and discharging behaviour of the SC design, regardless of the converter rated output.

TABLE 2. Specifications of the boost converter.

Parameters	Value
Inductance L	4.8 mH
Capacitance C1	22 µF
Input DC voltage	29V
Output voltage	200V
Duty Cycle	0.87
Switching frequency	50kHz

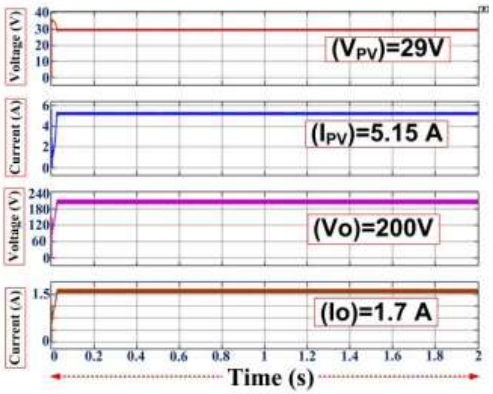


FIGURE 5. The solar PV and boost converter simulation waveforms.

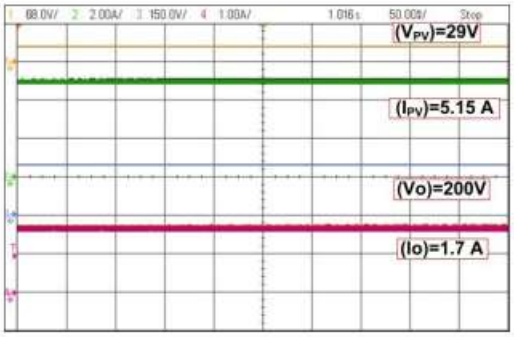


FIGURE 6. The solar PV and boost converter experimental waveforms.

The creation of different numbers of tiers of multilevel inverters is the outcome of adding multiple SC units. In this case, the SC units are cascaded to create MLI levels 17, 33, and 53. The subsequent subsections provide a design representation of the corresponding MLIs. The fundamental

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

unit of SC is shown in FIGURE 7(a). the charging and discharging actions of a solar cell. When connected in parallel to circumstances, the capacitor C charges to V1, and when connected in series to the source, it discharges to the load. These are the ideal conditions for the capacitor C to operate under. As stated,

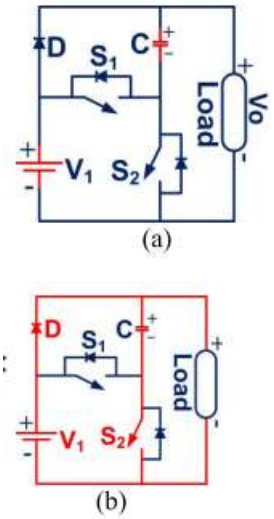


FIGURE 7. SCU (a) Basic SC unit: (b) Charging.

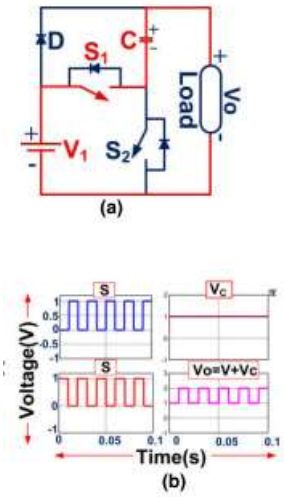


FIGURE 8. Capacitor in SC unit: (a) Discharging, (b) Simulation output.

Under ideal circumstances, as shown in FIGURES 7(a) & 8(a), the capacitor C Figures 7(b) and 8(a) depict is charged through the S2 switch at V0 = ±Vc1 for each half-cycle.

When the switch S1 at the front end of the suggested MLI architecture is in the conduction state, the discharging of the capacitor C begins. Both the switch S2 and diode Dare switched off throughout the discharge time. The load is powered by V1 and VC1, and each load's maximum current is known where

$$V_0 = V_1 + V_{C1} \quad (10)$$

The ideal value of SC for the obtained ripple voltages can be found during the discharging time. The waveform of the simulation output displayed in FIGURE 8(b).

If QC is the charge that C1 released during that time, then

$$Q_C = \int_{td1}^{td2} [I_0 sin\,(2\pi fst - \varphi)\,dt] \quad (11)$$

where fs is the fundamental frequency, I0 is the maximum output current, td1, td2 are the discharge periods, and ϕ is the phase difference between the voltage and current. The ripple voltage, or ΔVC, may be estimated using the angles found using

$$\Delta VC = \frac{1}{2\pi fsC} \int_{\theta}^{\pi-\theta} I0 \sin(2\pi fst - \varphi) d\omega t \quad (12)$$

where πθ is the angle at which the capacitor stops discharging and is the angle at which the capacitor discharges.

A. 17-LEVEL MLI

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

FIGURE 9 illustrates the design of a 17-level MLI with two SC units coupled in a cascade with fewer components. Ten controlled switches and two asymmetric DC sources without inductors make up the suggested MLI topology. Because of their different voltage levels, the two DC sources have an asymmetrical arrangement. This MLI topology reduces several power quality problems, including total standing voltage (TSV), cost factor, and cost per unit with different weight factor values, THD, switch count, component count level, and voltage stress.

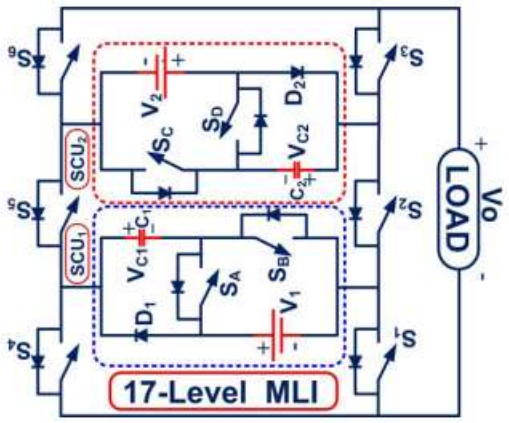


FIGURE 9. Developed structure of 17-level MLI.

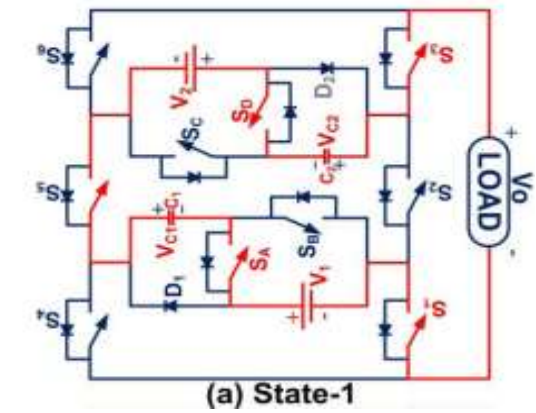
This topology is compared with other topologies and yields lower TSV. TABLE III shows the operation states and the path taken by the load current through the switches. FIGURE 10 depicts a few operating modes and switching pulses, whereas FIGURE 11 shows the anticipated output waveform.

The different modes of operation for the designed 17-level MLI are displayed in TABLE III. The switches SA, S5, SD, S3, and S1 activate to provide a load current route in mode-1 functioning of the circuit. Sources V1, VC1, V2, and VC2 act in the circuit and generate voltages of 50V, 150V, 50V, and 150V, respectively, to reach a maximum voltage of 400V. Table III shows the corresponding switching states, switching pulses, and current routes. When the circuit's V1, V2, and VC2 sources act and create voltages of 50V, 50V, and 150V, respectively, the switches D1, S5, SD, S3, and S1 turn on, resulting in a voltage of 7Vdc, or 350V. When operating in mode 3, the switches SD, S3, S6, S5, and V2 sources activate, creating a load current route where the circuit's voltages function as 50V and 150V, respectively, and provide a voltage of 6Vdc, or 300V.

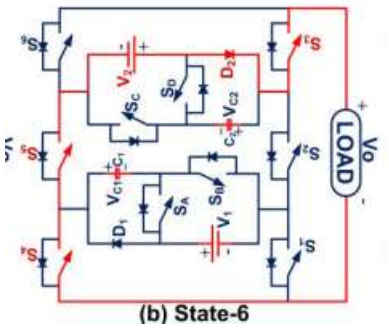
When operating in mode 4, the voltages V1, VC1, and V2 sources act in the circuit and cause the switches SA, S5, D2, S3, and S1 to turn on. These voltages produce voltages of 50V, 150V, and 50V, respectively, and result in a voltage of 5Vdc, or 250V. When operating in mode 5, the voltages V1 and V2 sources act in the circuit, causing the switches D1, S5, D2, S3, and S1 to turn on. This results in a voltage of 50V and 150V, respectively, and a voltage of 4Vdc equal to 200V. When operating in mode 6, the switches D2, S3, S4, S5, and V2 turn on when the voltage V2 source acts in the circuit, producing a 50V voltage and receiving a 3Vdc voltage, which is equivalent to 150V. When in mode 7, the voltages V1 and VC1 sources act in the circuit, causing the switches SA, S5, S6, and S1 to turn on. This creates a voltage of 50V and 150V, respectively, and a voltage of 2Vdc, which is equal to 100V. When operating in mode 8, the voltages V1 source act in the circuit and cause the switches D1, S5, S6, and S1 to turn on. This produces a voltage of 50V in each case and yields a voltage of Vdc, which is

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

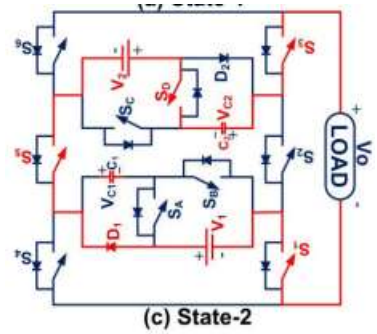
equivalent to 50V. When operating in mode-9, the switches S1, S2, and S3 turn on with no voltages acts in the circuit and produces a voltage of 0V.



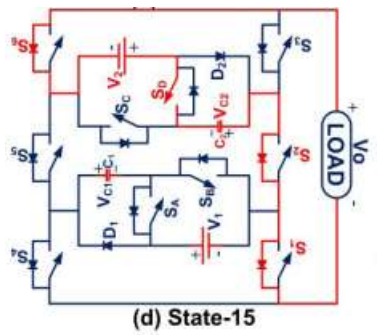
(a) State-1



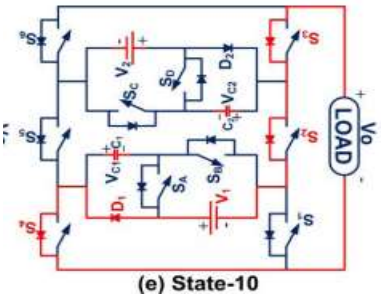
(b) State-6



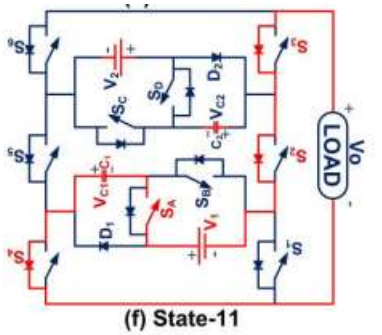
(c) State-2



(d) State-15



(e) State-10



(f) State-11

FIGURE 10. Modes of operation of the proposed 17-Level MLI topology.

Thus, a positive cycle is established. Together with the switching states listed in Table III, the negative modes of operation are used to implement the negative cycle. Consequently, the output waveform of the 17-level MLI is obtained with the 4.12% simulation THD displayed in FIGURE 14. The Figure 21's experimental THD is 4.12%, which is like that of THD simulation. The output waveform for the output Currents and voltage are displayed in FIGURES 12 and 13. Illustrations 14 and 15.

FIGURE 16 shows the output voltage and current of the experiment. When the MLI is tested using an R-load, 400V and 4A of voltage and current, respectively, are achieved. FIGURE 17 illustrates the outcome. The experimental result for the L-load is displayed in FIGURE 18, where the current and voltage are 6.8A and 400V, respectively. The outcome for RL-load is displayed in FIGURE 19. FIGURE 20 displays the experimental outcome for LR-

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

load. FIGURE 44 displays the entire setup for the experiment. Table VI displays the experimental parameters that were used to implement the 17-level MLI.

B. 33-LEVEL MLI

FIGURE 22 illustrates how two 17-level MLI units combined with fewer components are designed to create a 33-level MLI. The suggested MLI topology consists of four asymmetric DC sources and twenty controlled switches without inductors. The four DC sources are arranged asymmetrically because of their different voltage levels. Numerous problems with power quality, including total standing voltage (TSV), cost factor, and cost per unit with different THD, weight factor, switch count, and component values

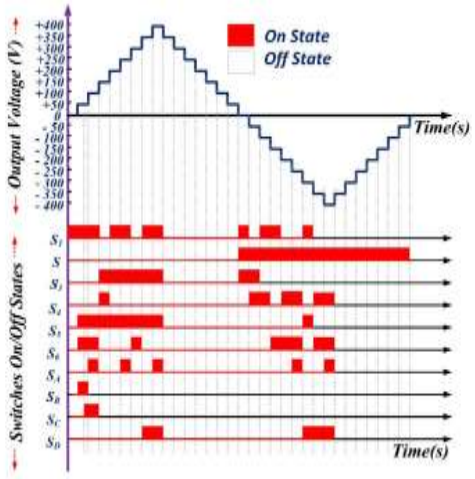


FIGURE 11. 17-Level expected output voltage waveform with switching pulses.

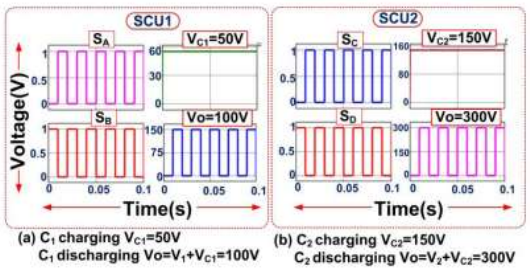


FIGURE 12. SCU Simulation output voltage waveforms of 17MLI.

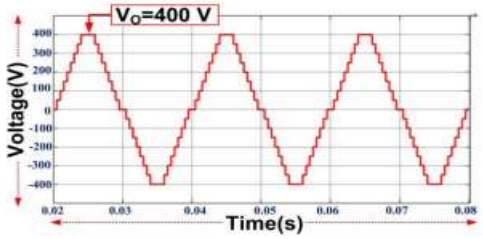


FIGURE 13. Simulation output voltage waveform of the 21-Level MLI.

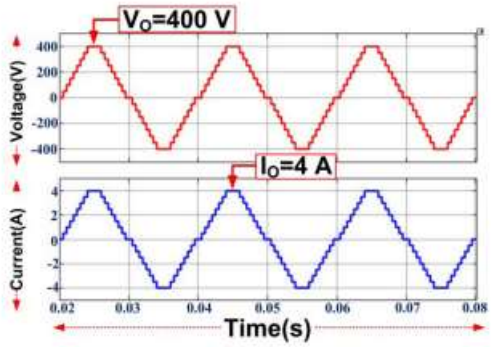


FIGURE 14. Simulation output voltage and current waveforms of the 17-Level MLI.

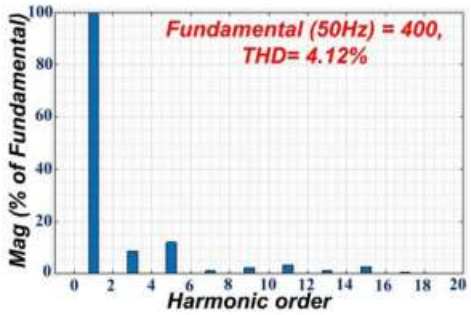


FIGURE 15. Simulation THD.

This MLI technology minimises voltage stress and count level. This topology is compared with other topologies and yields lower TSV. TABLE IV shows the stages of operation as well as the path taken by the load current through the switches. FIGURE 23 displays a few operating modes as well as the switching pulses.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

TABLE 3. Generation voltage levels according to Conduction of Switches of 17 MLI.

States	Load current path	Output Voltage (V)		
State-1	S_A, S_5, S_D, S_3, S_1	$8V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}$	+400
State-2	D_1, S_5, S_D, S_3, S_1	$7V_{dc}$	$V_1+V_2+V_{C2}$	+350
State-3	S_D, S_3, S_6, S_5	$6V_{dc}$	V_2+V_{C2}	+300
State-4	S_A, S_5, D_2, S_3, S_1	$5V_{dc}$	$V_1+V_{C1}+V_2$	+250
State-5	D_1, S_5, D_2, S_3, S_1	$4V_{dc}$	V_1+V_2	+200
State-6	D_2, S_3, S_4, S_5	$3V_{dc}$	V_2	+150
State-7	S_A, S_5, S_6, S_1	$2V_{dc}$	V_1+V_{C1}	+100
State-8	D_1, S_5, S_6, S_1	V_{dc}	V_1	+50
State-9	S_1, S_2, S_3	0	0	0
State-10	D_1, S_4, S_3, S_2	$-V_{dc}$	$-V_1$	-50
State-11	S_A, S_4, S_1, S_2	$-2V_{dc}$	$-(V_1+V_{C1})$	-100
State-12	D_2, S_2, S_1, S_6	$-3V_{dc}$	$-(V_2)$	-150
State-13	D_2, S_2, D_1, S_4, S_6	$-4V_{dc}$	$-(V_1+V_2)$	-200
State-14	D_2, S_2, S_A, S_4, S_6	$-5V_{dc}$	$-(V_1+V_{C1}+V_2)$	-250
State-15	S_D, S_2, S_1, S_5	$-6V_{dc}$	$-(V_2+V_{C2})$	-300
State-16	S_D, S_2, D_1, S_4, S_6	$-7V_{dc}$	$-(V_1+V_2+V_{C2})$	-350
State-17	S_D, S_2, S_A, S_4, S_6	$-8V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2})$	-400

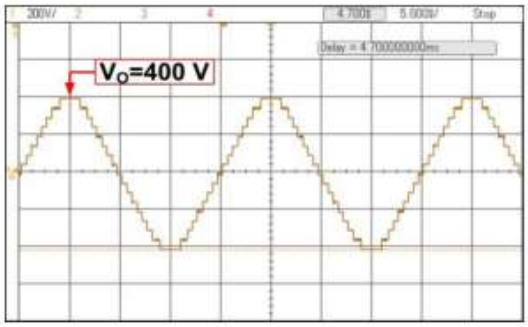


FIGURE 16. Experimental output waveform (Vo).

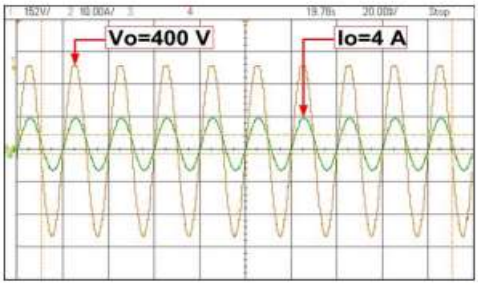


FIGURE 17. Experimental output waveform for R-load.

The different modes of operation for the designed 33-level MLI are displayed in TABLE IV. The switches SA, S5, SD, S3, S7, SE, S11, SH, S9, and S1 activate in mode-1 operation of the circuit, creating a load current path where sources V1, VC1, V2, VC3, V4, and VC4 act in the circuit and generate voltages of 25V, 25V, 75V, 75V, 25V, and 75V, respectively, to reach a maximum voltage of 400V. Table IV shows the corresponding switching pulses, switching states, and current routes. When operating in mode-2,

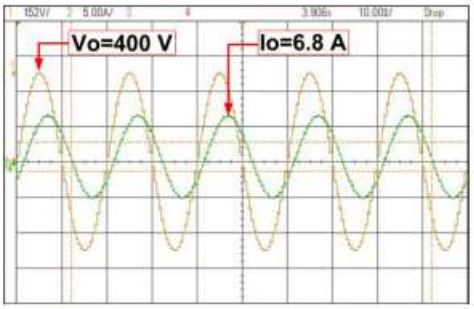


FIGURE 18. Experimental output waveform for L-load.

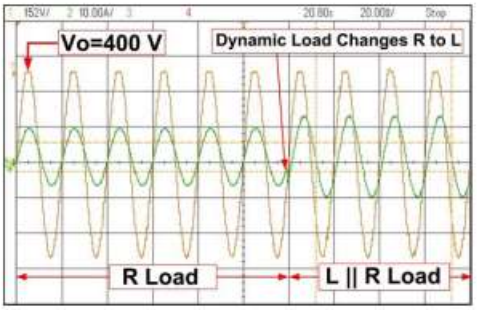


FIGURE 19. Experimental output waveform for R || L-load.

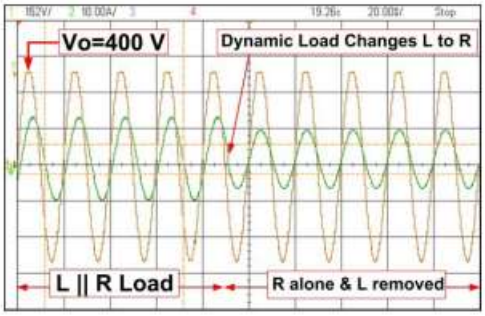


FIGURE 20. Experimental output waveform for L || R-load.

When V1, V2, VC2, V3, VC3, V4, and VC4 sources work in the circuit and create the voltages of 25V, 75V, 75V, 25V, and 75V respectively, the switches D1, S5, SD, S3, S7, SE, S11, SH, S9, and S1 turn on and yield a voltage of 15Vdc, which is equal to 375V. When operating in mode 3, the switches SD, S3, S7, SE, S11, SH, S9, S1, SB, SA, D1, S5, and VC4 sources function in the circuit, creating voltages of 75V, 75V, 25V, 25V, and 75V, respectively, and obtaining a voltage of 14Vdc equal to 350V. The switches SD, S3, S7, D3, S11, SH, S9, S1, SB, SA, and D3 operate in mode 4, enters the circuit and generates voltages of 75V, 75V, 25V, 75V, and 75V in that order. 13Vdc, or 325V, is the result. When operating in mode 5, the voltages V2, VC2, V4, and VC4 sources work in the circuit and create a voltage of 75V, 75V, 75V, and 75V accordingly, and the switches SD, S3, S7, SF, SE, D3, S11, SH, S9, S1, SB, SA, D1, S5, and so on. 300V is equal to 12Vdc. When operating in mode 6, the voltage V1, VC1, V2, VC2, and V4 sources work in the circuit and create a voltage of 25V, 25V, 75V, 75V, and 75V accordingly. This voltage is then converted to 11Vdc, or 275V, by the switches SA, S5, SD, S3, S7, SF, SE, D3, S11, D4, S9, and S1. When operating in mode-7, the voltages V1, V2, VC2, and V4 sources act in the circuit and generate a voltage of 25V, 75V, 75V, and 75V accordingly. This voltage is then converted to 10Vdc, or 250V, by turning on the switches D1, S5, SD, S3, S7, SF, SE, D3, S11, S4, S9, and S1. When operating in mode 8, the switches D2, S3, S7, SF, SE, and V2, VC2, and V4 sources operate in the circuit to generate voltages of 75V, 75V, and 75V, respectively, and 9Vdc. This comes to 225V. When operating in mode-9, the switches turn on SA, S5, SD, S3, S7, S8, S9, and S1 using voltages V1. A voltage is produced in the circuit by VC1, VC2, and VC2 correspondingly, 25V, 25V, 75V, and 75V, to obtain a voltage of 8Vdc. 200V is equivalent. When operating in mode-10, the switches D1, S5, turn on SD, S3, S7, S8, S9, and S1 using voltages V1, V2, and VC2 functions in the circuit to provide a 25V voltage, 75V and 75V correspondingly and obtain a 7Vdc voltage, which is equivalent to 175V. When operating in mode-11, the voltages V2 are applied to the switches SD, S3, S7, S8, S9, S1, SB, SA, D1, and S5 and VC2 functions in the circuit to generate a 75V voltage respectively, to obtain a voltage of 6Vdc, which is equivalent to 150 V. When operating in mode-12, the switches SA, S5, D2, S3, S7, S8, S9, and S1 activate using voltages V1, VC1, and V2, operates in the circuit to generate a voltage of 25 volts, 25 volts and 75V, respectively, to obtain an equivalent voltage of 5Vdc up to 125V. When operating in mode-13, the switches SA, S5, S6, S7, SE, S11, S12, and S1 activate at voltages of V1, VC1, and V3. and VC3 operate in the circuit, producing voltages of 25, 25, 25, and 25 volts, respectively, thus obtaining a voltage of 4 Vdc, or 100 V. When operating in mode 14, the voltages V2 acts in the circuit, producing a voltage of 75V, and the switches D2, S3, S7, S8, S9, S1, SB, SA, D1, S5 turn on with the voltages V2 acts in the circuit, producing a voltage of 3Vdc, which is equal to 75V. When operating in mode-15, the voltages V1 and VC1 act in the circuit, causing the switches SA, S5, S6, S7, S8, S9, and S1 to turn on. This produces a voltage of 25V and 25V, respectively, and results in a voltage of 2Vdc equal to 50V. When operating in mode-16, the switches D1, S5, S6, S7, S8, S9, and S1 Turn on one voltage source.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

When V1 operates in the circuit, it generates a voltage of 25V and receives a voltage of Vdc, which is the same as 25V. Thus, a positive cycle is created. Together with the switching states listed in Table IV, the negative modes of operation are used to implement the negative cycle. As a result, FIGURE 26's 33-level MLI output waveform is produced with a simulation THD of 2.54%. The experimental THD, which is like the simulation THD, is displayed in FIGURE 32 at 2.54%. Figures 24 and 25 display the output waveforms for output voltage and current. When the MLI is tested with an R-load, 400V and 4A of voltage and current are obtained, respectively and FIGURES 27 & 28 display the outcome that was reached. FIGURE 29 displays the experimental result for Lload. where the current is 6.8A and the voltage is 400V, respectively. The outcome for RL-load is displayed in FIGURE 30. The experimental result for LRload is displayed in FIGURE 31. TABLE V and FIGURE 44 display the whole experimental configuration and specs.

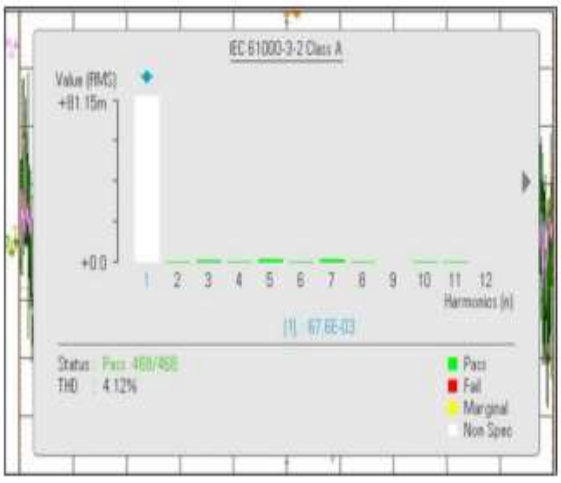


FIGURE 21. Experimental THD.

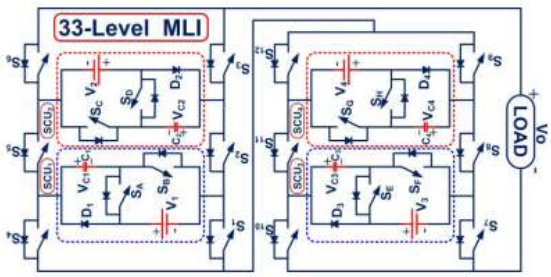


FIGURE 22. Developed structure of 33-level MLI.

C. 53-LEVEL MLI

FIGURE 33 illustrates the construction of a 53-level MLI using a combination of three SC units coupled with fewer components. Except for inductors, the suggested MLI topology consists of 14 controlled switches and three asymmetric DC sources. The three DC sources are arranged asymmetrically because of their different voltage levels. This MLI strategy minimises several power quality issues, including total standing voltage (TSV), cost factor, and cost per unit with different weight factor values, THD, switch count, component count level, and voltage stress. This topology is compared with other topologies and yields lower TSV. Table VI shows the states of operation as well as the path taken by the load current through the switches. FIGURE 34 shows a few operating modes as well as the switching pulses. There are several ways to run the constructed 53-level MLI, which are displayed in TABLE VI. To create a load current path during mode-1 operation of the circuit, the switches SE, S2, SA, S7, SD, S4, S5, and VC1 turn on. These sources act in the circuit to produce voltages of 15.4V, 15.4V, 46.2V, 46.2V, 138.6V, and 138.6V, respectively, to reach a maximum voltage of 400.4V. Switching pulses that correspond to each other. Table V shows the states and current routes. To

create a load current route and achieve a maximum voltage of 385V, the circuit's mode 2 operation involves the switches SE, S2, D1, S7, SD, S4, S5, and VC3 turning on. These sources act in the circuit to produce voltages of 15.4V, 46.2V, 46.2V, 138.6V, and 138.6V, respectively. When operating in mode 3, the circuit's switches SE, S2, SB, SA, D1, S7, SD, S4, S5, and VC3 sources activate, creating a load current route where the circuit's voltages of 46.2V, 46.2V, 138.6V, and 138.6V, respectively, are produced, leading to a maximum voltage of 369.6V. When operating in mode 4, the circuit's switches SE, S2, SA, S7, D2, S4, S5, and VC1 sources activate, creating a load current route where the circuit's voltages of 15.4V, 15.4V, 46.2V, 138.6V, and 138.6V, respectively, are produced, leading to a maximum voltage of 354.2V. During the circuit's mode-5 operation, the switches SE, S2, D1, S7, D2, S4, S5, and VC3 turn on to provide a load current route. The sources V1, V2, V3, and VC3 act on the circuit to produce voltages of 15.4V, 46.2V, 138.6V, and 138.6V, respectively, to reach a maximum voltage of 338.8V. When the V3 source works in the circuit and generates a voltage of 138.6V, the switches D3, S2, S3, S4, S5, and S5 turn on. This results in a voltage of 9Vdc, which is equal to 138.6V. The switches D1, S6, S5, S4, S3, and S3 activate in mode-28 operation, creating a load current route where the -V1 source acts in the circuit, producing a voltage of -15.4V and receiving a voltage of -Vdc equal to -15.4V. When in mode-53 operation, the voltages V1, VC1, V2, VC2, V3, and VC3 sources act in the circuit and cause the switches SD, S3, SA, S6, SE, S1, S8, and VC3 to turn on. This results in a voltage of 26 Vdc and voltages of 15.4 V, 15.4 V, 46.2 V, 46.2 V, 138.6 V, and 138.6 V, respectively. This is 400.4V in equivalent. Thus, a positive cycle is created. Together with the switching states listed in Table VI, the negative modes of operation are used to implement the negative cycle.

As a result, FIGURE 37's 53-level MLI output waveform is produced with a simulation THD of 1.41%. FIGURE 43 displays the experimental THD, which is 1.41%, like the simulation THD. Figures 35 and 36 display the output waveforms for output voltage and current. When the MLI is tested with an R-load, 400V and 4A of voltage and current are obtained, respectively, and FIGURES 38 & 39 display the outcome that was reached. FIGURE 40 displays the experimental result for Lload. where the current is 6.8A and the voltage is 400V, respectively. The outcome for RL-load is displayed in FIGURE 41. The experimental result for LR load is displayed in FIGURE 42. The whole experimental configuration and details are displayed in Table V and FIGURE 44.

D. TOTAL STANDING VOLTAGE (TSV)

The circuit's switches are chosen in large part based on the total standing voltage (TSV). This represents the total of all blocking voltages for all semiconductor devices in the topology.

VSbi = Vi and VSuni = 2Vi are the voltage stresses on the bi-directional and unidirectional switches, respectively.

Industrial Engineering Journal
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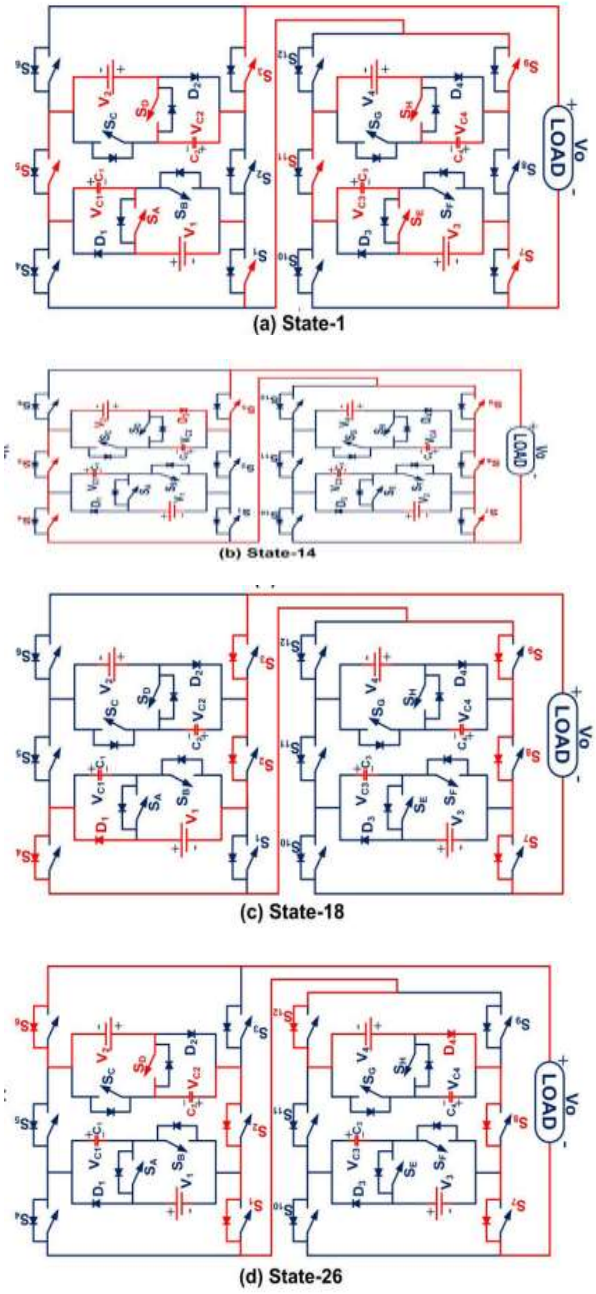


FIGURE 23. Modes of operation of the proposed 33-Level MLI topology.

TABLE 4. Generation voltage levels according to Conduction of Switches of 33 MLI.

States	Load current path	Output Voltage (V)		
State-1	$S_{11}, S_9, S_{10}, S_6, S_5, S_2, S_{12}, S_8, S_7, S_1$	$16V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}+V_3+V_{C3}+V_4+V_{C4}$	+400
State-2	$D_3, S_9, S_{10}, S_6, S_5, S_2, S_{12}, S_8, S_7, S_1$	$15V_{dc}$	$V_1+V_2+V_{C2}+V_3+V_{C3}+V_4+V_{C4}$	+375
State-3	$S_{11}, S_9, S_5, S_{10}, S_{12}, S_8, S_7, S_6, S_2, D_4, S_1$	$14V_{dc}$	$V_1+V_{C1}+V_3+V_{C3}+V_4+V_{C4}$	+350
State-4	$S_{11}, S_9, S_5, D_4, S_{12}, S_8, S_7, S_6, S_2, D_4, S_1$	$13V_{dc}$	$V_1+V_{C1}+V_3+V_4+V_{C4}$	+325
State-5	$S_{11}, S_9, S_5, S_{12}, D_4, S_{12}, S_8, S_7, S_6, S_2, D_4, S_1$	$12V_{dc}$	$V_1+V_{C1}+V_4+V_{C4}$	+300
State-6	$S_{11}, S_9, S_{10}, S_5, S_{12}, S_8, D_4, S_{12}, D_4, S_6, S_1$	$11V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}+V_4$	+275
State-7	$D_3, S_9, S_{10}, S_5, S_{12}, S_8, D_4, S_{12}, S_6, S_6, S_1$	$10V_{dc}$	$V_1+V_2+V_{C2}+V_4$	+250
State-8	$D_3, S_9, S_{10}, S_5, D_4, S_{12}, D_4, S_8, S_7, S_6, S_6, D_4, S_1$	$9V_{dc}$	$V_1+V_{C2}+V_4$	+225
State-9	$S_{11}, S_9, S_{10}, S_{12}, S_5, S_8, S_6, S_1$	$8V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}$	+200
State-10	$D_3, S_9, S_{10}, S_{12}, S_5, S_8, S_6, S_1$	$7V_{dc}$	$V_1+V_2+V_{C2}$	+175
State-11	$S_{11}, S_9, S_5, S_{12}, S_5, S_{10}, S_6, D_4, S_1$	$6V_{dc}$	V_1+V_{C2}	+150
State-12	$S_{11}, S_9, D_3, S_{12}, S_5, S_8, S_6, S_1$	$5V_{dc}$	$V_1+V_{C1}+V_2$	+125
State-13	$S_{11}, S_9, S_{10}, S_5, S_8, S_{12}, S_6, S_1$	$4V_{dc}$	$V_1+V_{C1}+V_{C2}+V_{C3}$	+100
State-14	$D_3, S_9, S_{12}, S_5, S_8, S_{12}, S_6, D_4, S_1$	$3V_{dc}$	V_2	+75
State-15	$S_{11}, S_9, S_{10}, S_5, S_{12}, S_8, S_6, S_1$	$2V_{dc}$	V_1+V_{C1}	+50
State-16	$D_3, S_9, S_{10}, S_{12}, S_5, S_8, S_6, S_1$	V_{dc}	V_1	+25
State-17	$S_{11}, S_9, S_{10}, S_5, S_{12}, S_8$	0	0	0
State-18	$D_3, S_9, S_{10}, S_5, S_{12}, S_8, S_6, S_1$	$-V_{dc}$	$-V_1$	-25
State-19	$S_{11}, S_9, S_{10}, S_5, S_{12}, S_8, S_6, S_1$	$-2V_{dc}$	$-(V_1+V_{C1})$	-50
State-20	$D_3, S_9, S_{10}, S_5, S_{12}, S_8, S_6$	$-3V_{dc}$	$-V_2$	-75
State-21	$S_{11}, S_9, S_{10}, S_5, S_{12}, S_{10}, S_6, S_1$	$-4V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2})$	-100
State-22	$D_3, S_9, S_{10}, S_5, S_{12}, S_{10}, S_6, S_1$	$-5V_{dc}$	$-(V_1+V_{C1}+V_{C2})$	-125
State-23	$S_{11}, S_9, S_{10}, S_5, S_{12}, S_{10}, S_6$	$-6V_{dc}$	$-(V_1+V_{C1})$	150
State-24	$S_{11}, S_9, D_3, S_{12}, S_5, S_{10}, S_6, S_1$	$-7V_{dc}$	$-(V_1+V_2+V_{C2})$	-175
State-25	$S_{11}, S_9, S_{10}, S_4, S_5, S_{10}, S_6, S_1$	$-8V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2})$	-200
State-26	$S_{11}, S_9, S_{10}, S_{12}, D_4, S_{10}, S_6, S_1$	$-9Vdc$	$-(V_1+V_{C2}+V_4)$	-225
State-27	$S_{11}, S_9, D_3, S_{12}, S_{12}, D_4, S_{10}, S_6, S_1$	$-10Vdc$	$-(V_1+V_2+V_{C2}+V_4)$	-250
State-28	$S_{11}, S_9, S_{10}, S_{12}, S_{12}, D_4, S_{10}, S_6, S_1$	$11V_{dc}$	$-(V_1+V_{C2}+V_2+V_{C2}+V_4)$	-275
State-29	$S_{11}, S_9, S_{10}, S_{12}, S_{10}, S_{10}, S_6, S_1$	$12V_{dc}$	$-(V_1+V_{C2}+V_4+V_{C4})$	-300
State-30	$S_{11}, S_9, S_{10}, S_{12}, S_{10}, S_{10}, D_4, S_{10}, S_6$	$13V_{dc}$	$-(V_1+V_{C2}+V_2+V_4+V_{C4})$	-325
State-31	$S_{11}, S_9, S_{10}, S_{12}, S_{10}, S_{10}, S_{10}, S_6$	$14V_{dc}$	$-(V_1+V_{C2}+V_2+V_{C2}+V_4+V_{C4})$	-350
State-32	$S_{11}, S_9, D_3, S_{12}, S_{10}, S_{10}, S_{10}, S_6$	$15V_{dc}$	$-(V_1+V_2+V_{C2}+V_2+V_{C2}+V_4+V_{C4})$	-375
State-33	$S_{11}, S_9, S_{10}, S_{12}, S_{10}, S_{10}, S_{10}, S_6$	$16V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2}+V_2+V_{C2}+V_4+V_{C4})$	-400

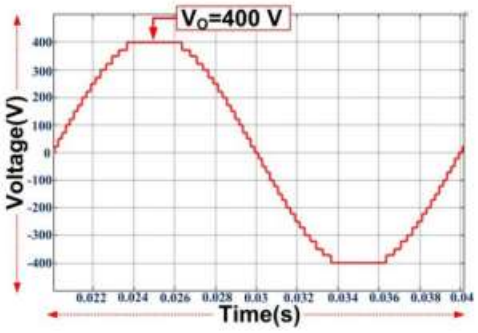


FIGURE 24. Simulation output voltage waveform of the 33-Level MLI.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

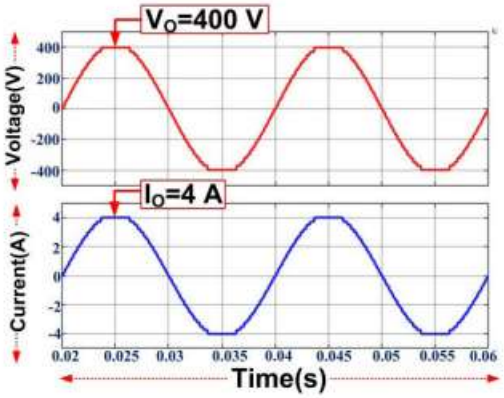


FIGURE 25. Simulation output voltage and current waveforms of the 33-Level MLI.

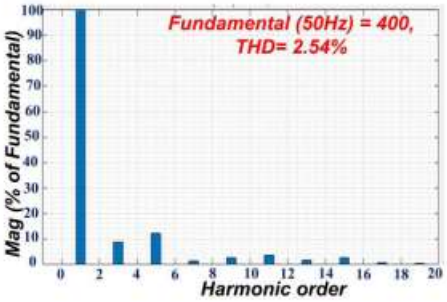


FIGURE 26. Simulation THD.

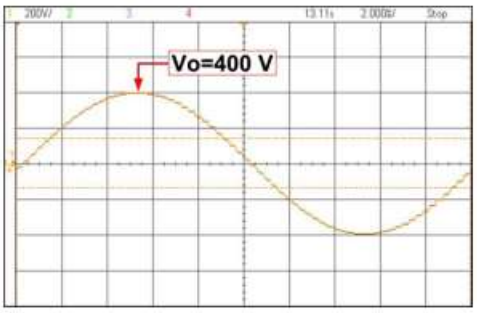


FIGURE 27. Experimental output waveform (Vo).

where i = 1, 2.... n, and n are the complimentary switches count, respectively. For the suggested topology, the maximum output voltage (Vo) is Vo, max = 400V. In the proposed MLI, the voltages are equal for complementing switches, and all switches are unidirectional. TSV is therefore computed using the relationship below:

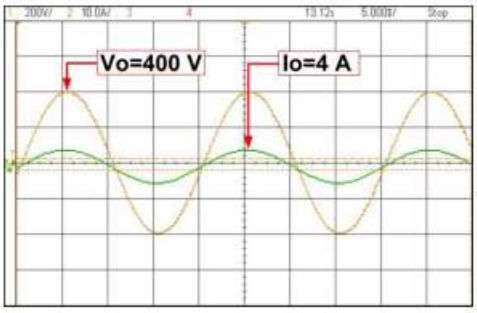


FIGURE 28. Experimental output waveform for R-load.

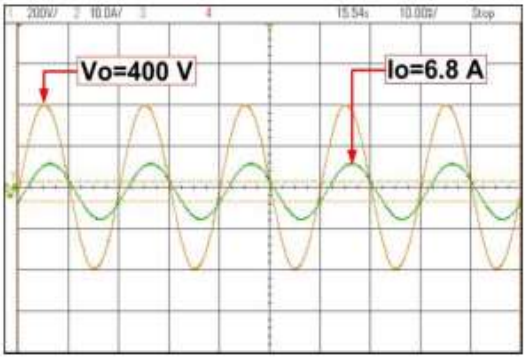


FIGURE 29. Experimental output waveform for L-load.

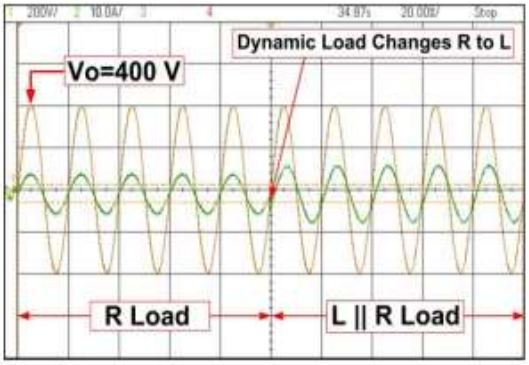


FIGURE 30. Experimental output waveform for R || L-load.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

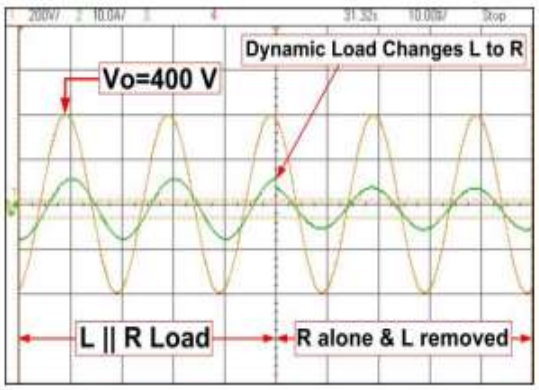


FIGURE 31. Experimental output waveform for L || R-load.

$$TSV = 2(V_{S1} + V_{S3} + \ldots\ldots\ldots\ldots V_{S(2n+1)}) \quad (13)$$

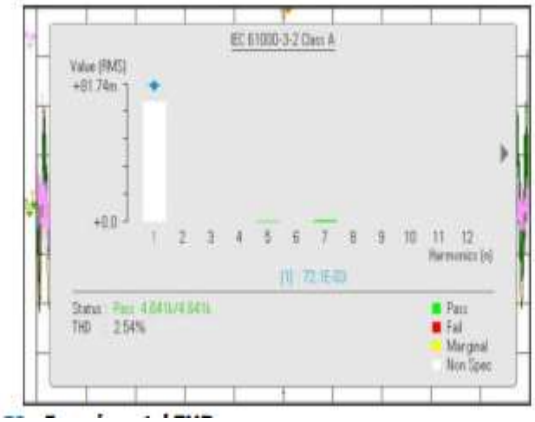


FIGURE 32. Experimental THD.

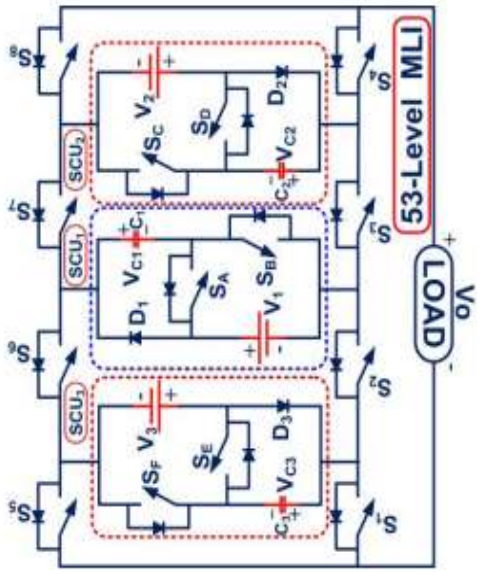
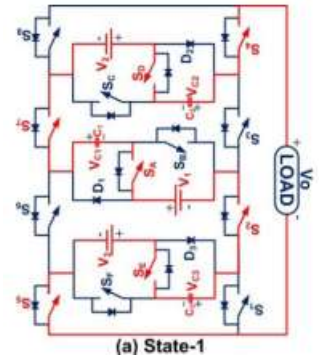
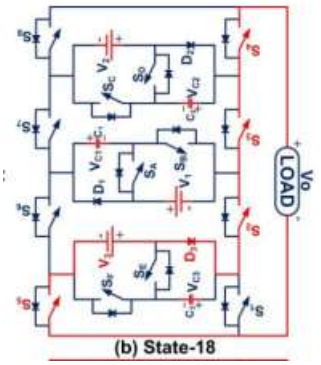
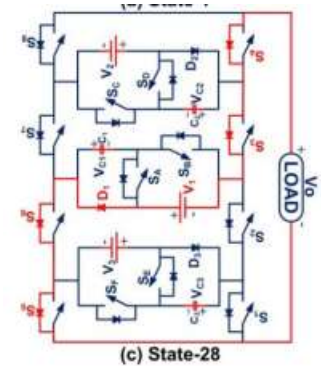


FIGURE 33. Proposed 53-Level MLI.







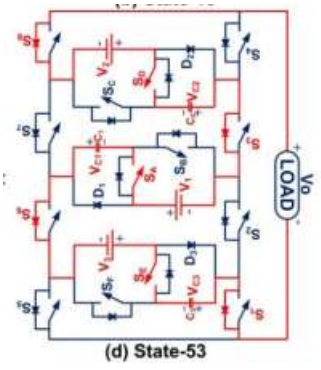


FIGURE 34. Modes of operation of the proposed 53-Level MLI topology.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

TSV may be computed using equation (7) for the created 17-level MLI, and it is determined to be 16Vdc. Similarly, TSV is determined to be 50Vdc for the 33-level MLI and 30.8Vdc for the planned 53-level MLI.

TABLE 5. Specifications of 53-level MLI.

Output Voltage V_o	400V
Output current I_o	4A
dSPACE controller	RTI1104
Resistive load (Lamp)	100Ω
Inductive load	98Mh
IGBT	IGBT CM75DU-12, 600V, 75A
Motor load	Single-phase, 230V, 0.5HP

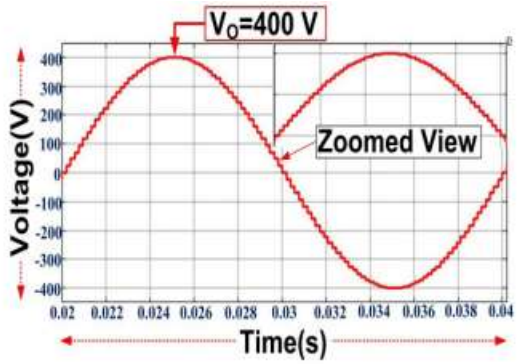


FIGURE 35. Simulation output voltage waveform of the 53-Level MLI.

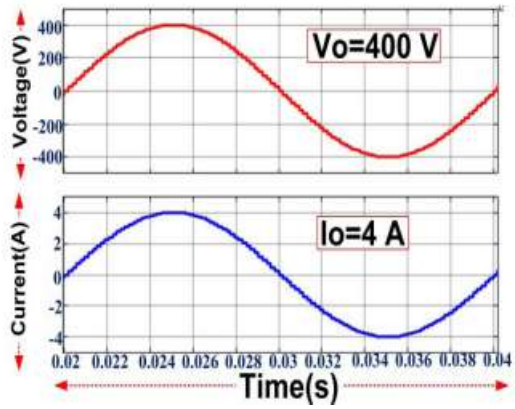


FIGURE 36. Simulation output voltage and current waveforms of the 53-Level MLI.

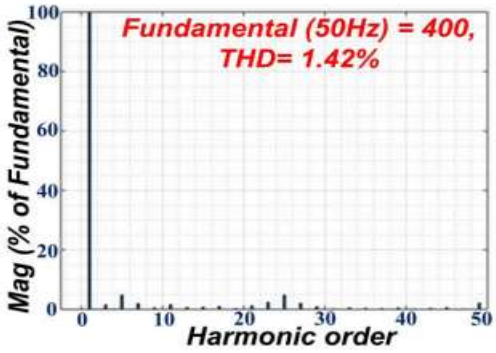


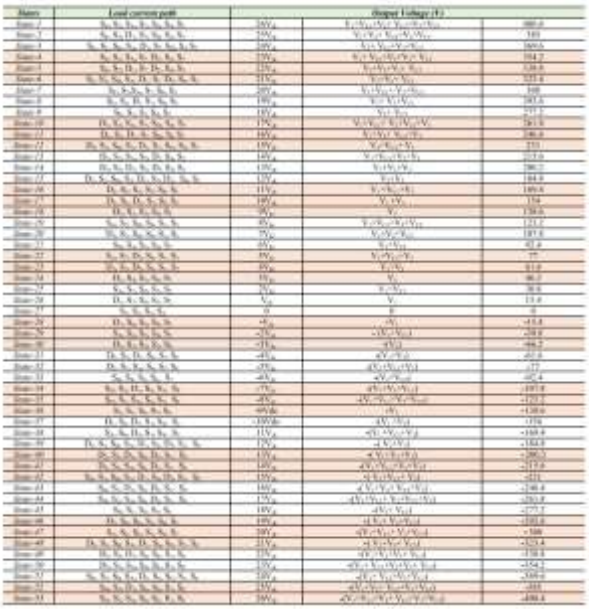
FIGURE 37. Simulation THD.

E. COST FUNCTION

Equation (14) [37] can be used to compute the cost factor for the proposed 53-level MLI by considering various characteristics such as the number of switches, sources, total standing voltage, and driver circuits.

$$CF = (N_S + N_{dk} + N_d + N_c + \alpha TSV_{pu}) \times n \quad (14)$$

TABLE 6. Generation voltage levels according to Conduction of Switches of 53 MLI.



where NS is the number of switches, Ndk is the number of gate driver circuits, Nd is the number of diodes, and Nc is the number of capacitors. The maximum

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

standing voltage for conduction switches is known as TSV. The total standing voltage per unit, or TSVpu, is determined by

$$TSV(pu) = V_{TSV}/V_{omax} \quad (15)$$

where n is the circuit's count of DC sources. The weight coefficient, represented by α, is multiplied by TSVpu. The cost function is computed using the relation, and the inverter architecture with no diodes or capacitors can be ignored.

$$CF = (S + N_{dk} + \alpha TSV_{pu}) \times n \quad (16)$$

TABLE 7. Cost comparison of various multilevel inverters with proposed 17-Level MLI.

Components required		[39]	[40]	[41]	[42]	[43]	[44]	Proposed
Number of Switches (Ns)		16	14	10	20	18	20	16
Number of diodes (Nd)		16	20	10	20	12	20	12
Number of capacitors (Ncap)		4	4	0	0	0	0	2
DC sources (n)		4	8	4	8	2	8	2
Driver board circuits (Ndk)		14	14	10	20	10	20	10
Components count per level (Fcol)		5.17	5.57	3	4	2	4	1.53
Total Standing Voltage (TSV)		11	22	36	36	40	36	16
Total harmonic distortion (THD)		-	-	7.1	5.7	-	4.12	4.23
CF/N_{Level}	α=0.5	3.5	4.17	4.94	5.05	5.18	4.97	2
	α=1.5	4.16	5.47	9.18	7.17	9.88	2.94	2.94

TABLE 8. Variance of various 33-Level MLI topologies.

Components required		NPC	FC	CHB	[45]	[46]	[47]	[48]	Proposed
Number of Switches (Ns)		64	64	20	18	21	79	20	20
Number of diodes (Nd)		32	0	20	18	32	0	20	4
Number of capacitors (Ncap)		32	0	16	0	16	15	0	4
DC sources (n)		32	32	5	1	1	1	8	4
Driver board circuits (Ndk)		64	64	20	18	21	79	20	20
Components count per level (Fcol)		6.78	4.84	2.12	1.84	2.75	9.27	2.08	1.47
Total Standing Voltage (TSV)		64	64	84	60	68	55	72	50
Total harmonic distortion (THD)		-	-	-	-	-	-	5.2	2.54
Cost Function/Levels (CF/L)	α=0.5	8.84	4.9	2.81	1.9	2.81	5.37	2.12	1.62
	α=1.5	8.96	5.0	2.63	2.0	2.93	5.45	2.26	1.71

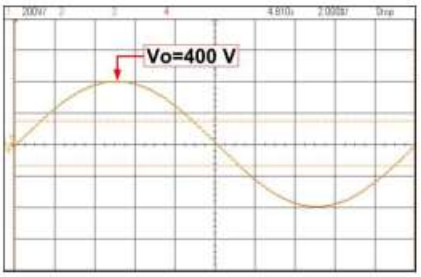


FIGURE 38. Experimental output waveform (Vo).

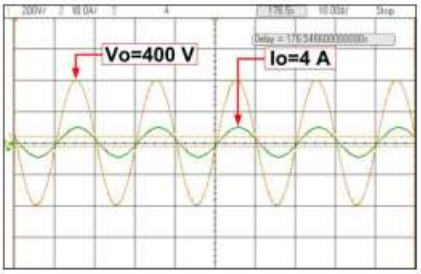


FIGURE 39. Experimental output waveform for R-load.

It is important to think about the value of α in a way where one value is larger than one and the other is smaller than one. In this study, the cost function evaluation yields a value of 1.5 (>1) for α, when the actual value is 0.5 (<1). Any MLI's cost-effectiveness is determined using level count (CF/L). It is necessary to compute this value for both values.

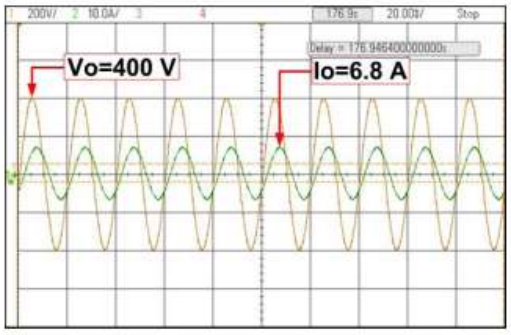


FIGURE 40. Experimental output waveform for L-load.

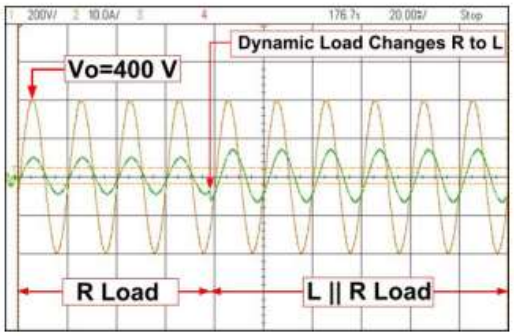


FIGURE 41. Experimental output waveform for R || L-load.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

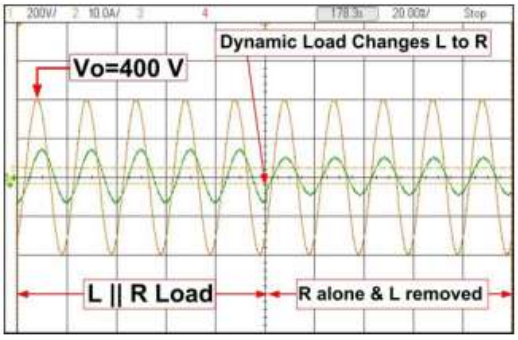


FIGURE 42. Experimental output waveform for L || R-load.

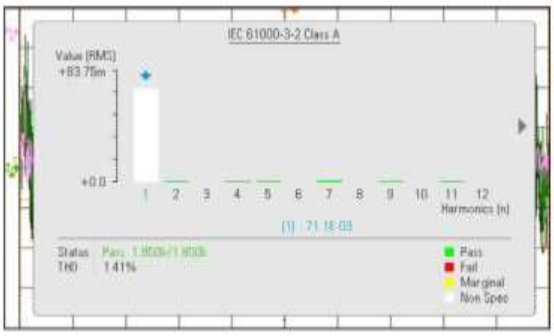


FIGURE 43. Experimental THD.

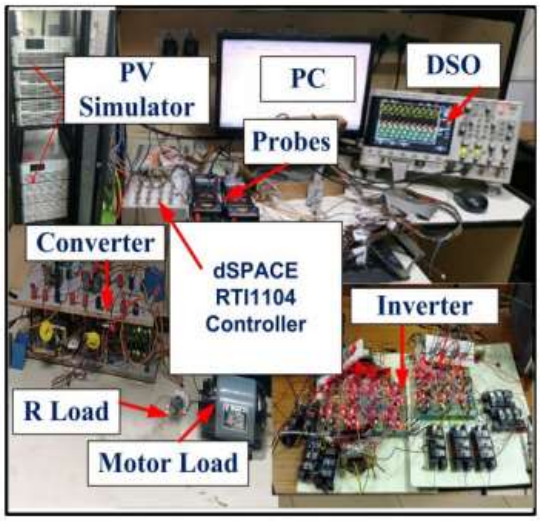


FIGURE 44. Experimental setup.

utilised within a circuit. Less components are used when the value is lower, which results in lower losses and more efficiency.

The following relationship is used to calculate the component count per level factor Fccl:

$$F_{ccl} = \frac{N_s + N_d + N_c + N_{dk} + n}{N_{Lev}} \quad (17)$$

It is discovered that the component count level factors for the 33-level MLI, the created 17-level MLI, and the suggested 53-level MLI are, respectively, 1.53, 1.57, and 0.69.

TABLE 9. Cost comparison of various multilevel inverters with proposed 53-Level MLI.

Components required		NPC	FC	CHB	[49]	[50]	Proposed
Number of levels N_l		53	53	53	49	42	53
Number of Switches (Ns)		104	104	32	12	12	14
Number of diodes (Nd)		52	0	0	0	0	3
Number of capacitors (Ncap)		52	52	8	4	3	3
DC sources (n)		52	52	8	2	3	3
Driver board circuits (Ndk)		104	104	32	12	12	14
Components count per level (Fccl)		6.86	5.88	1.5	0.61	0.66	0.69
Total Standing Voltage (TSV)		104	104	104	34	32	30
Total harmonic distortion (THD)		-	-	-	0.7	1.5	1.41
Cost Function/Levels (CF/L)	α=0.5	6.9	5.92	1.54	0.62	0.73	0.7
	α=1.5	6.98	6.0	1.62	0.65	0.76	0.73

F. POWER LOSS AND EFFICIENCY

Conduction and switch-related switching losses make up the total losses. Equation (18) can be used to determine the switches' conduction losses.

$$P_{Cls} = \left[V_S + R_S i^{\beta}(t)\right] i(t) \quad (18)$$

where Vd represents the voltage drop of the diodes and VS is the voltage drop of the IGBT switch. The equivalent resistance (RS) of the switch and the equivalent resistance (Rd) of the diode are the same. Equation (12) provides the generalised relation for calculating conduction power losses (Pcl) while considering the NIGBT

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024

switches and Nd diodes at a given point in time.

$$P_{Cl} = \frac{1}{2\pi}\int_0^{2\pi}\left[N_{IGBT}(t)\,P_{cl,IGBT}(t)\,dt\right] \quad (19)$$

Equation (13) can be used to compute the switching losses.

$$P_{Sl} = f\sum_{K=1}^{N_{switch}}\left[\sum_{j=1}^{N_{on,k}} En_{on,kj} + \sum_{j=1}^{N_{off,k}} En_{off,kj}\right] \quad (20)$$

which represent the energy that the switches use, Aeon and Eoff.

Calculating the overall power losses (Ptotal loss)

$$P_{total\ loss} = P_{cl} + P_{sl} \quad (21)$$

This relationship is used to compute the efficiency (η):

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (22)$$

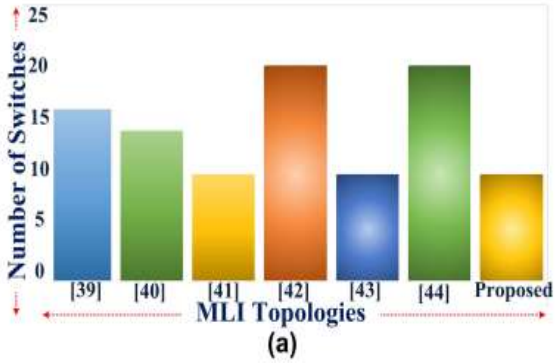
where the input and output powers are denoted by Pin and Pout.

Estimating the output power is possible:

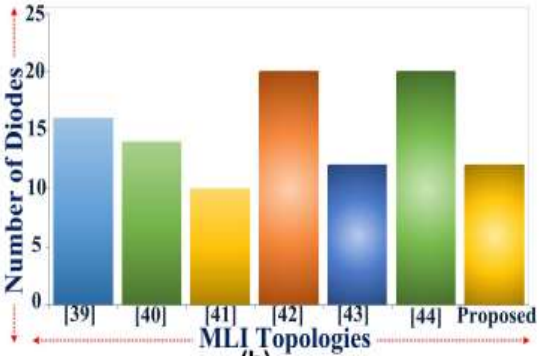
$$P_{out} = V_{rms} * I_{rms} \quad (23)$$

IV. COMPARISON STUDIES

Based on the different factors stated below, a comparison may be made for the developed 17-level, 33-level, and proposed 53-level MLIs. It is seen that, for both values of α, the designed 17-level MLI topology is more economical when compared to the various contemporary topologies. The suggested MLI is contrasted with several existing topologies considering crucial elements like the quantity of switches,



(a)



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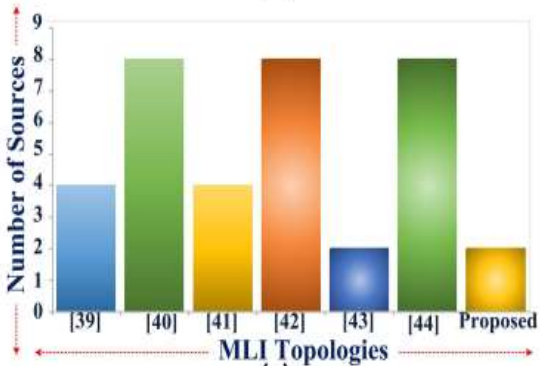

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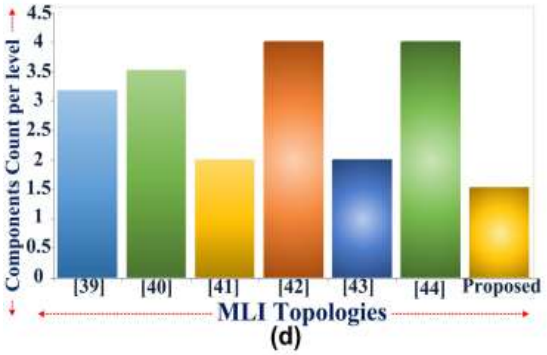

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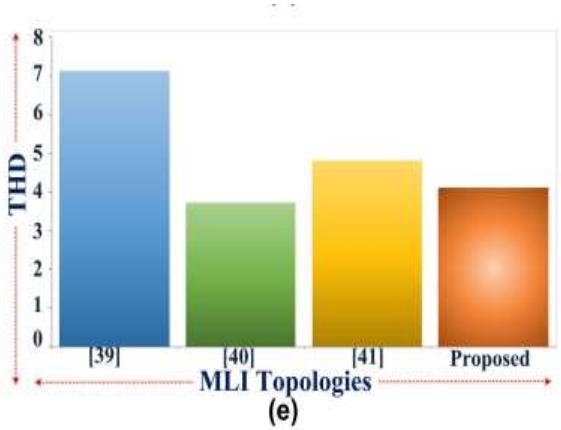
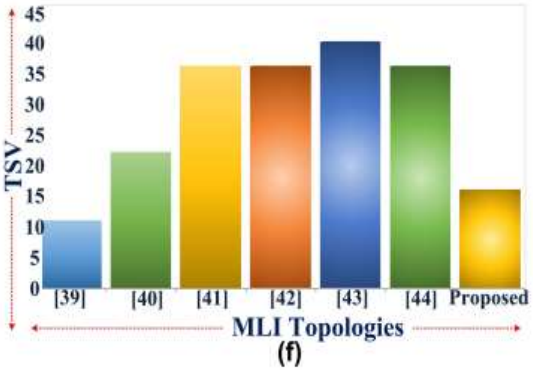
Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024





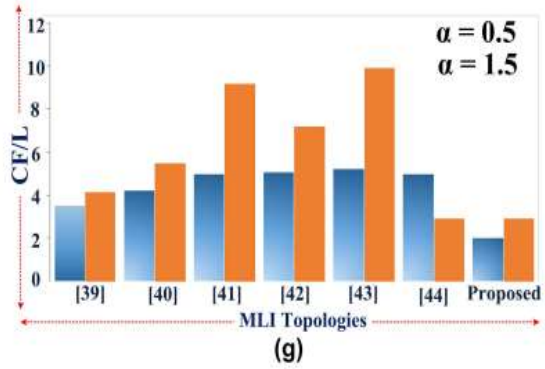
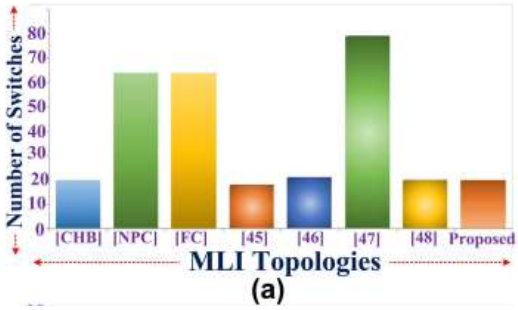
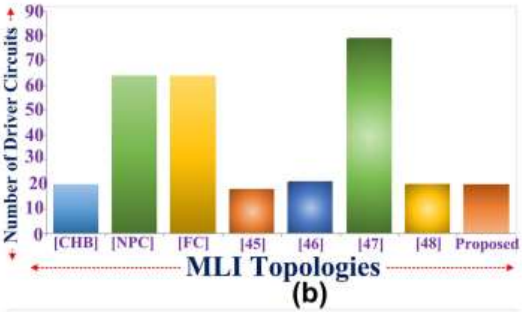
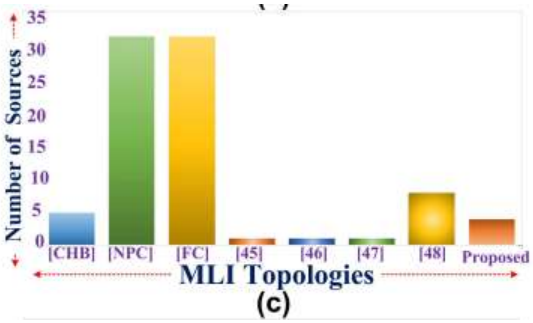


FIGURE 45. Comparison of various 17-Level MLI topologies (a) Switches count (b) Diodes count (c) DC sources count (d) Components count per level (e) THD (f) TSV (g) Cost function/Level count.

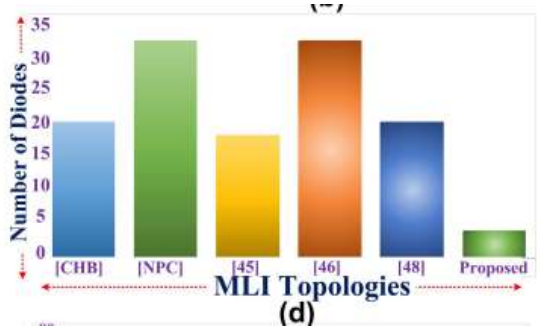
Table VII and FIGURE 45 show the number of DC sources, gate driver circuits, capacitors, total standing voltage, and components per level. The full standing voltage comparison is shown in FIGURE 45(f), where it is lower than for the other topologies. The cost function comparison for different topologies is shown in FIGURE 45(g), where cost-effectiveness is determined. Additionally, the 33-level MLI is contrasted with the previously described characteristics, which are shown in Table VIII and visually displayed in Figure 46. The cost function comparison for different topologies is shown in Figure 46(i), where it is determined to be cost-effective. When the suggested 53-level MLI is compared to several topologies of varying levels, it is observed that, for both values of α, this topology is more affordable than the numerous contemporary topologies. The suggested MLI is contrasted with several existing topologies considering crucial elements like the quantity of switches,

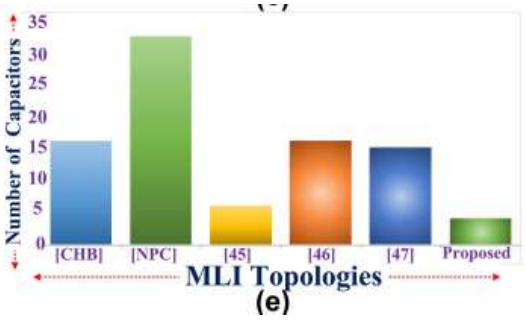


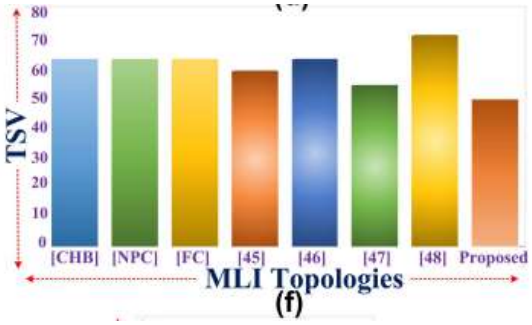


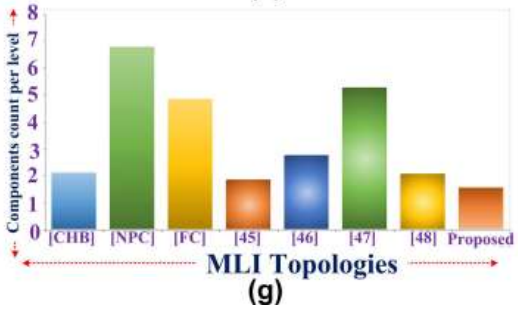


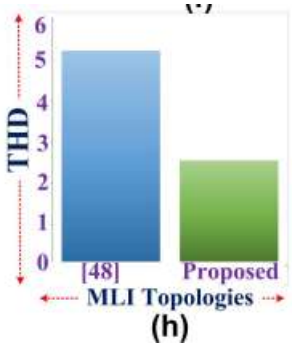
Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 11, November : 2024











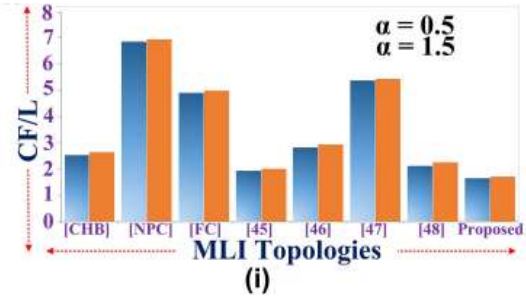
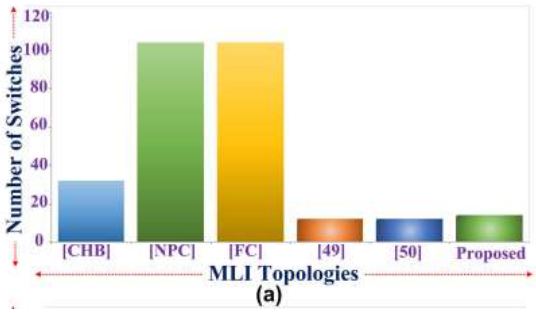


FIGURE 46. Comparison of various 33-Level MLI topologies. Switches count (b) Gate driver circuits count (c) DC sources count (d) Diodes count (e) Capacitors count (f) TSV (g) Components count per level (h) THD (I) Cost function/Level count.

The total standing voltage, DC source count, gate driver circuits, capacitor count, and total standing voltage are shown graphically in FIGURE 47 (d), which compares the whole standing voltage and is lower than the other topologies. These data are found in TABLE IX. The cost function comparison for different topologies is shown in FIGURE 47(I), where it is determined to be cost-effective. In every comparative parameter, the suggested MLI produced superior results.



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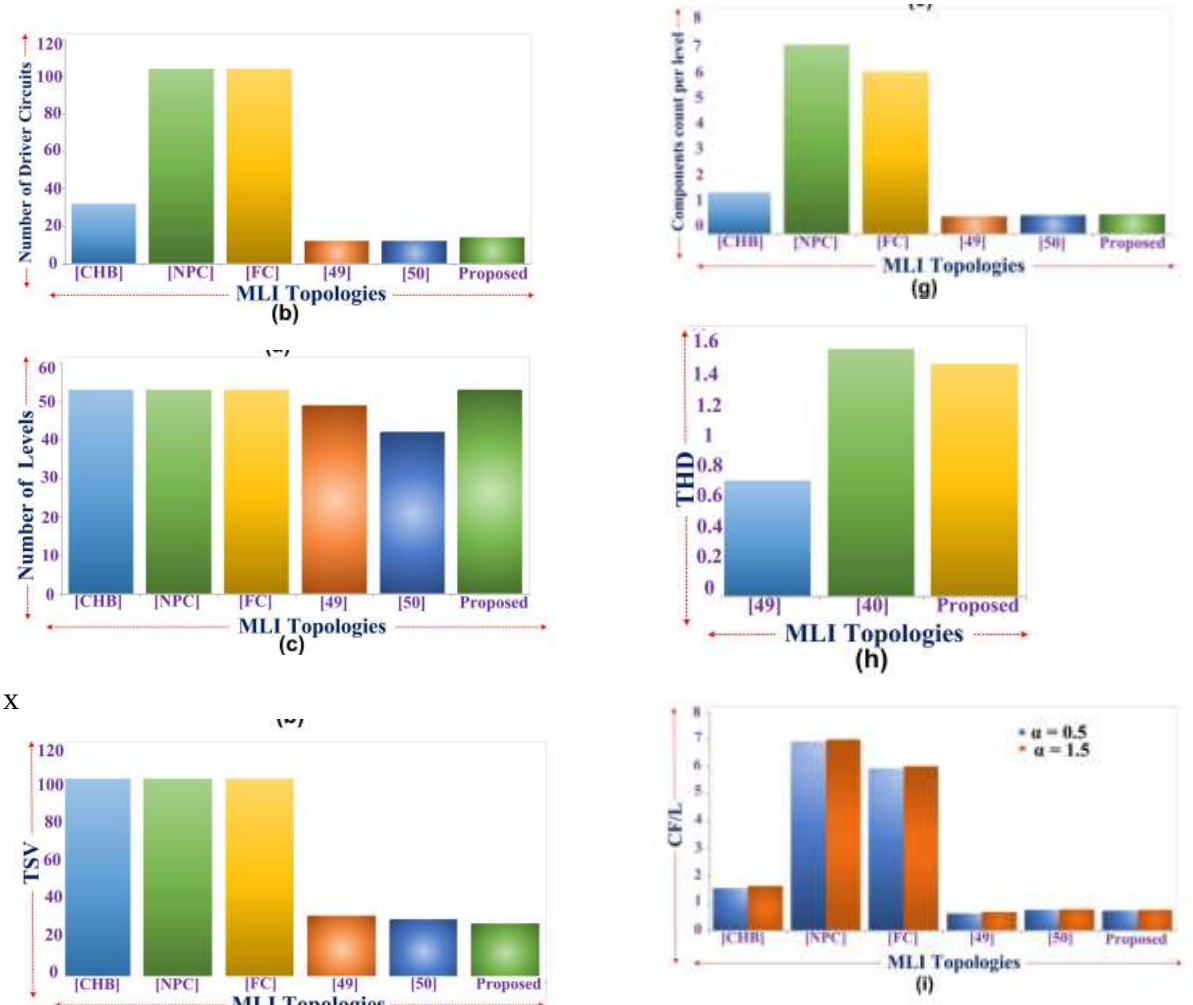

FIGURE 47. Comparison of various topologies of MLI with different levels with proposed 53-Level MLI Switches count (b) Gate driver circuits count (c) Number of levels (d) TSV (e) DC sources count (f) Capacitors count (g) Components count per level (h) THD (I) Cost function/Level count.

V.CONCLUSION

To improve efficiency and reliability while lowering the cost and size of the inverter, the 53-level MLI topology for electric car applications is devised and implemented for solar PV energy systems using fewer semiconductor components. When the P&O algorithm-based MPPT technique is applied, a stable result is produced

regardless of the situation. The suggested MLI is put into practise using different sets of SC connections. An MLI configuration with 17 levels is produced by cascading a basic two-unit design. Two 17-level MLIs cascade together to generate a 33-level MLI, while three SC units' cascade together to create the proposed 53-level MLI. Every MLI is created and contrasted using different topologies according to several factors, including the number of devices, TSV, THD, and cost function per level count. The comparison analysis demonstrates that the suggested MLI has lower power losses and is more efficient. It is observed that the experimental and simulated THD are 1.41%. With a TSVpu of 1.15, efficiency of 94.21%, and CF/L values of 0.7 and 0.73 for both choices of α, it is evident that the cost is much lower than with other topologies. Testing is done on the suggested MLI with various dynamic load variations. Applications related to renewable energy are best suited for this topology.

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