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GDI BASED COMPARATOR REDUNDANCY FOR RELIABLE AND STOCHASTIC FLASH ADC

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Abstract:

A digital comparator is constructed from two cross-coupled 3-input digital NAND gates, and designed in tanner EDA along with inbuilt amplifier stages. Regarding amplifier a highly efficient fully differential trans conductance amplifier, based on several input-to-output paths is designed. Some traditional techniques, such as positive feedback, nonlinear tail current sources, and current mirror-based paths, are combined to increase the trans conductance, thus leading to larger dc gain and higher gain bandwidth (GBW) product. Two flipped voltage-follower (FVF) cells are employed as variable current sources to provide class-AB operation and adaptive biasing of all other drivers. The proposed structure includes several input-to-output paths that play the role of dynamic current boosters during the slewing phase, thus improving the slew rate (SR) performance.

Keywords: Fully differential, operational trans conductance amplifier (OTA), positive feedback, slew rate (SR), trans conductance, class-AB, slew rate (SR), gain bandwidth (GBW).

Introduction: In these and other applications, operational transconductance amplifiers (OTAs) are widely employed as active elements in switched-capacitor filters, data converters, sample and hold circuits, or as buffer amplifiers for driving large capacitive loads [1]. Besides low-voltage and power-efficient operation, these OTAs should have a fast settling response, not limited by slew rate. Conciliating all these requirements is difficult with conventional (class A) OTA topologies, since the bias current limits the maximum output current LOW-VOLTAGE operation and optimized power-to-performance ratio are required by modern wireless and portable electronics in order to decrease battery weight and size and to extend battery lifetime. In these and other applications, operational trans conductance amplifiers (OTAs) are widely employed as active elements in switched-capacitor filters, data converters, sample and hold circuits, or as buffer amplifiers for driving large capacitive loads [1]. Besides low-voltage and power-efficient operation, these OTAs should have a fast settling response, not limited by slew rate. Conciliating all these requirements is difficult with conventional (class A) OTA topologies, since the bias current limits the maximum output current. Operational trans conductance amplifiers (OTAs) are widely used in integrated circuits, including switched-capacitor circuits, voltage regulators, and biomedical circuits as a fundamental building block [1], [2]. The folded cascode (FC) structure is usually one of the best choices for low-voltage, single-stage OTA, where high dc gain and large-signal swing are required [3], [4]. Some advantages, such as lower flicker noise, lower input common-mode level, and higher nondominant poles, can also be achieved if pMOS devices are used at the input differential pair [3], [5]. However, the accuracy of mixed-mode circuits and systems, in which an OTA-based integrator or buffer is used, directly depends on the OTA's specifications. In other words, the speed and the large-signal step response are influenced by the slew rate (SR), gain bandwidth (GBW), and dc gain that affect the accuracy, for example, of an analog-to-digital converter [1]. To increase the efficiency of the conventional FC amplifier, the recycling FC (RFC) amplifier was presented in [3] and [6] achieving double GBW and dc gain. The RFC structure attracted the attention of

many circuit designers to further improve its performance by employing idle devices as new drivers [7], dynamic current boosting paths [8], double recycling structure [5], transconductance enhancing method [9], [10], [11], [12], positive feedback [1], [13], and quasi-floating gate method [14]. Although all the abovementioned techniques improved the performance of the conventional amplifiers, some of them suffer from a class-A operation that limits the SR performance. Indeed, a constant tail current source delivers the same current for both small- and large-signal operations, which certainly limits the dynamic current when a large signal is applied to the input. To remove this limitation, flipped voltage-follower (FVF)-based differential structures [15], [16] were used [17], [18] to provide a variable tail current source by which the dynamic current can be increased, depending on the input signal amplitude. It also provided a situation under which the circuit was adaptively biased that caused a class-AB operation during slewing phase. Nonetheless, these techniques limit the frequency response of the OTA, because of more input-to-output paths, resulting in a lower phase margin. Therefore, designing and implementing high-gain and high-speed OTAs in CMOS technology with low expenses in power consumption and die area are still a challenge that circuit designers are dealing with. In this brief, two FVF cells are used as two nonlinear tail current sources with the capability of increasing the dynamic currents under large-signal operation, causing a high SR performance. It means that two FVF-based differential structures are configured, by which some idle devices, pMOS load transistors, are adaptively biased as new drivers, resulting in an enhancement in the small-signal transconductance too. Due to the use of an additional path taken from the FVF cells again, the nMOS load transistors are also used as new drivers to reincrease the transconductance. Employing these techniques causes a class-AB operation that significantly improves the driving capability of the circuit such that a high SR is achieved. In addition, a positive feedback circuit is added to the nMOS current mirrors, thus improving both dc and transient characteristics. Combining the abovementioned techniques not only enhances the circuit performance but also results in very low expenses in power consumption and die area; thus, such a combination could be one of the best choices among other efficient structures.

Existing method:

FVF-Based Differential Structure: Fig. 1 shows the FVF-based differential structure that was realized by adding the transistor M1a to the FVF cell composed of M1b and M3a [15]. Due to the low output resistance of the FVF circuit and

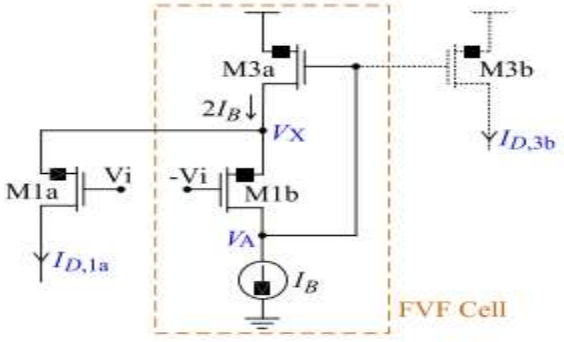

Fig. 1. FVF-based differential structure.

improved accuracy, we can assume that the ac voltage at node X (Vx) is approximately equal to Vi , (Vi ≈ VX). Therefore, a kind of differential input signal (+Vi and −Vi) is applied to the gate and source terminals of M1a, causing two times enhancement in the transconductance for a short-circuit current at the drain of M1a, (ID,1a/Vi) ≈ −2gm,1a. Another advantage of this structure could be its unity voltage

gain between the input and node A ($V_A/V_i \approx -2g_{m,1a}/g_{m,3a}$). Indeed, if both M1a and M1b are biased by the same current IB, the input signal appears at node A with a gain of 1; thus, it can easily be mirrored to the output load, through M3b, for further transconductance enhancement, $(I_{D,3b}/V_i) \approx -g_{m,3b}$. Regarding large-signal operation, the FVF cell plays the role of a variable tail current source for both transistors M1a and M3b such that when the amplitude of the input signal is increased, the output currents $I_{D,1a}$ and $I_{D,3b}$ are nonlinearly increased [15]. Assuming operation in strong inversion region, the current $I_{D,1a}$ can be expressed by

$$I_{D,1a} = \frac{\beta_{1a,b}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1a,b}}} + V_{id}\right)^2 \qquad (1)$$

Proposed Topology Fig. 2(a) shows the structure of the proposed OTA in which transistors M1a and M2a are basic drivers that can be found in all FC-based topologies. Unlike a conventional OTA, transistors M1a and M2a are biased by two nonlinear current sources, created by FVF cells, thus providing two FVF-based differential structures. Note that since the input signal is applied to both gate and source terminals of the basic drivers M1a and M2a, achieving a double transconductance is expected. In addition, the idle pMOS load transistors, M3c and M4c, are adaptively driven by M3a and M4a, respectively. Consequently, M3c and M4c operate as additional drivers, further increasing the small-signal transconductance of the OTA. In a similar way, two additional paths are created by M3b and M4b to drive the idle nMOS load transistors M7c and M8c too. To achieve this goal, two nMOS diode-connected topologies, M7a and M8a, are employed to form two current mirrors, M7a:M7c and M8a:M8c. Thus, the input signal is also applied to the gate terminals of M7c and M8c as two new drivers resulting in further transconductance enhancement. Due to the application of partial positive feedback circuit, created by cross-coupled transistors M7d and M8d, another enhancement in the transconductance is achieved [1]. The positive feedback increases the impedance seen from nodes C and D, thus increasing the amplitude of ac signal at these nodes and consequently increasing the small-signal transconductance of the OTA. Such an enhancement can efficiently be reused by adding another path through M7b and M8b, which causes the fifth transconductance enhancement. Thus, considering all the above effects, the small-signal transconductance of the proposed OTA is expressed by

$$G_m \approx 2g_{m,1a} + g_{m,3c} + \frac{g_{m,3b}}{g_{m,7a} - g_{m,7d}}\left(g_{m,7c} + g_{m,7b}\right) \qquad (2)$$

where $g_{m,i}$ represents the transconductance of transistor Mi. Assuming the same overdrive voltage, Vod, for all transistors, it can be considered that $g_{m,3a} = 2(g_{m,1a})$, $g_{m,3c} = q(g_{m,3a})$, $g_{m,3b} = s(g_{m,3a})$, $g_{m,7d} = k(g_{m,7a})$, $g_{m,3b} = (1 + k)g_{m,7a}$, $g_{m,7b} = m(g_{m,7a})$, and $g_{m,7c} = n(g_{m,7a})$. Thus, (1) is simplified to

$$G_m = 2\left[1 + q + s\frac{n+m}{1-k}\right]g_{m,1a}$$

where parameters m, n, k, s, and q represent the current gains of the current mirrors, denoted in Fig. 2. For this design, their values were chosen equal to 1, 3.5, 0.5, 0.75, and 2.75 [to avoid latchup or unstable behavior in the proposed amplifier, (1 − k) is set to 0.5]. Thus, substituting the above values results in $G_{m,proposed} = 27g_{m,1a}$ that shows about 600% enhancement in the transconductance compared to the conventional FC amplifier, $G_{m,conventional} = 4g_{m,1a}$ [3]. Since GBW and dc gain have a direct

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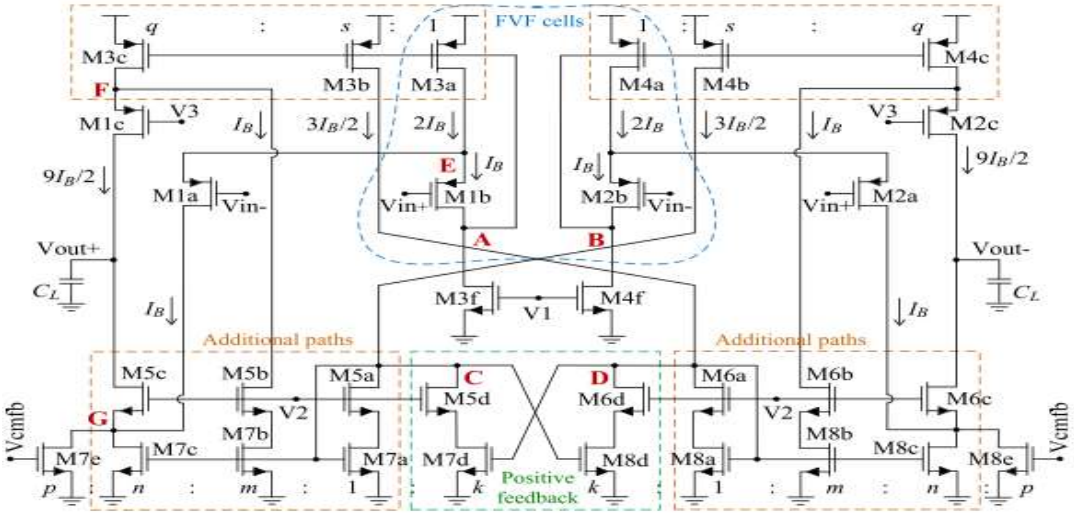
relationship with the transconductance, these two parameters will show a significant enhancement. However, the proposed OTA consumes 2IB more than a conventional FC structure for M7e–M8e and the positive feedback topology causing a 12% increment in its power dissipation. To evaluate the large-signal performance, Fig. 2(b) shows the behavior of the proposed circuit when two large positive and negative signals are applied to Vin− and Vin+, respectively. Thus, transistors M1a and M2b, shown in dashed lines, turn off, forcing M4f into the deep triode region. It means that the voltages at nodes A and C are increased and voltages at nodes B and D are decreased. Consequently, the dynamic currents flowing through transistors M2c, M4c, M4b, M5a, M7a, M7c, and M5c, shown in red lines, are significantly increased. Fortunately, the currents flowing through other paths are decreased or limited by constant current sources, M3f and M8e, such that the output capacitive loads are charged or discharged by a single dynamic path with a boosted current. In other words, since the voltages at source terminals of M1c and M6c are, respectively, decreased and increased, these two transistors turn off and the positive and negative output loads are, respectively, discharged and charged by approximately the same boosted current flowing through M5c and M2c. Such a benefit not only increases the SR but also provides a symmetric positive and negative SR for a large input step. According to the large-signal current of M3b by ID,3b = ID,4b = s(IB + ID,1a), the SR of the OTA is given as

$$\mathrm{SR} = \frac{q\left[I_B + \frac{\beta_{1a}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1a}}} + V_{id}\right)^2\right] - \frac{I_B}{2}}{C_{L,\,out^-}} + \frac{n\left(s\left[I_B + \frac{\beta_{1a}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1a}}} + V_{id}\right)^2\right] - \frac{I_B}{4}\right) + I_B}{C_{L,\,out^+}} \quad (4)$$

where $I_B/2$ in the first term and $I_B/4$ and I_B in the second term of (4) are biasing currents of M8b, M7d, and M7e, respectively. Considering $q = 2.75$, $n = 3.5$, $s = 0.75$, and $C_{L,\text{out}+} = C_{L,\text{out}-} = C_L$ the SR is simplified to

$$\mathrm{SR} \approx \frac{4I_B}{C_L} + 3\frac{\beta_{1a}\left(\sqrt{\frac{2I_B}{\beta_{1a}}} + V_{id}\right)^2}{C_L}. \quad (5)$$



(a)

Fig. 2. (a) Proposed multipath fully differential amplifier

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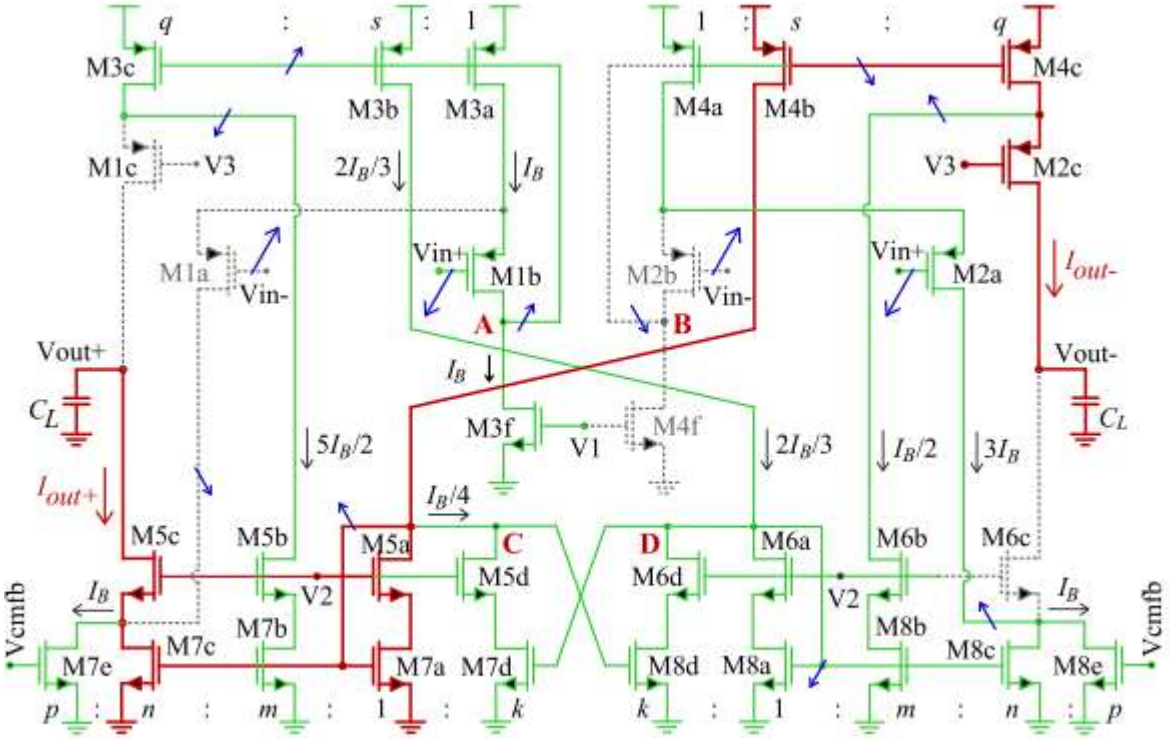
In comparison with the conventional FC amplifier with an SR of 8IB/CL [3], (4) shows that a higher SR is achieved for the proposed OTA. This is because the FVF-based differential structures significantly increase the driving capability of the proposed OTA. The FVF cells act as variable biasing sources responsible for the term of 3 ×β1a[√(2IB/β1a) + Vid] 2 in (5) such that the slewing current will increase for large input amplitude, thus improving the speed of charging/discharging of the load capacitance CL. In fact, the FVF-based differential structures not only increase the small-signal transconductance but also provide a class-AB operation under largesignal conditions. Although the main performance metrics of the proposed circuit are improved, the additional input-to-output paths affect the frequency response of the OTA, introducing additional parasitic poles and zeros.



(b)

(b) Large-signal behavior of the proposed OTA.

It is seen from Fig. 2(a) that the input signal passes through six nodes, including A, C, E, F, G, and output such that four of them (A, C, E, F) are new, compared to the conventional FC OTA [3]. However, the poles associated with nodes A and C are located at lower frequencies than other new poles; therefore, their impact is dominant. Considering the gate–source capacitance, CGS, as the dominant parasitic capacitance of MOS transistor, ωA and ωC can be approximated by

$$\omega_A \cong -\frac{g_{m,3a}}{(1+s+q)\,C_{GS,3a}} \qquad (6)$$

$$\omega_C \cong -\frac{g_{m,7a}-g_{m,7d}}{(1+n+m+k)\,C_{GS,7a}}. \qquad (7)$$

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Proposed Method:

Reconfigurable Comparator using GDI and FVF based OTA:

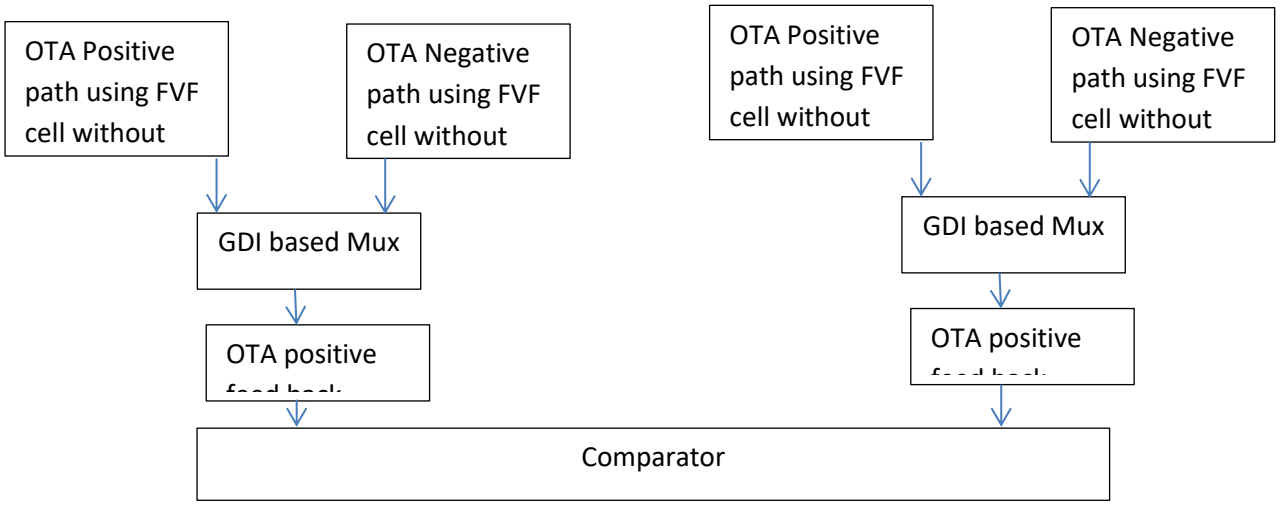

Fig3: Reconfigurable cooperator using proposed method

Comparator Circuit: A comparator circuit compares two voltages and outputs either a 1 (the voltage at the plus side; VDD in the illustration) or a 0 (the voltage at the negative side) to indicate which is larger. Comparators are often used, for example, to check whether an input has reached some predetermined value. In most cases a comparator is implemented using a dedicated comparator IC, but op-amps may be used as an alternative. Comparator diagrams and op-amp diagrams use the same symbols.

Figure shows a comparator circuit. Note first that the circuit does not use feedback. The circuit amplifies the voltage difference between Vin and VREF, and outputs the result at Vout. If Vin is greater than VREF, then voltage at Vout will rise to its positive saturation level; that is, to the voltage at the positive side. If Vin is lower than VREF, then Vout, will fall to its negative saturation level, equal to the voltage at the negative side.

In practice, this circuit can be improved by incorporating a hysteresis voltage range to reduce its sensitivity to noise.

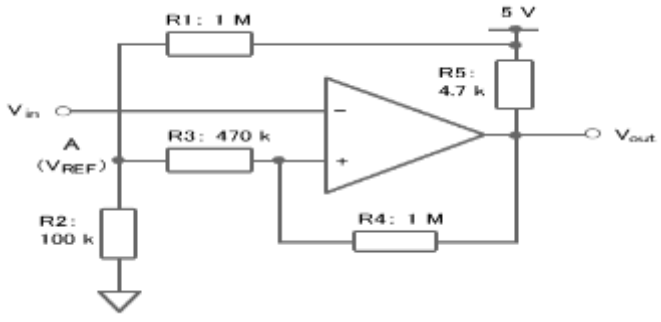

Figure 4: Comparator Circuit with Hysteresis

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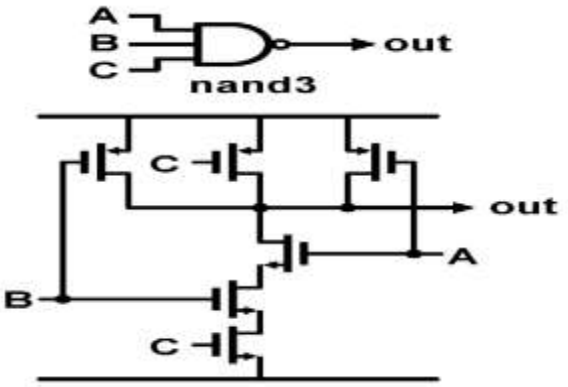

Fig.5 A standard digital CMOS NAND3 gate and its internal transistor schematic

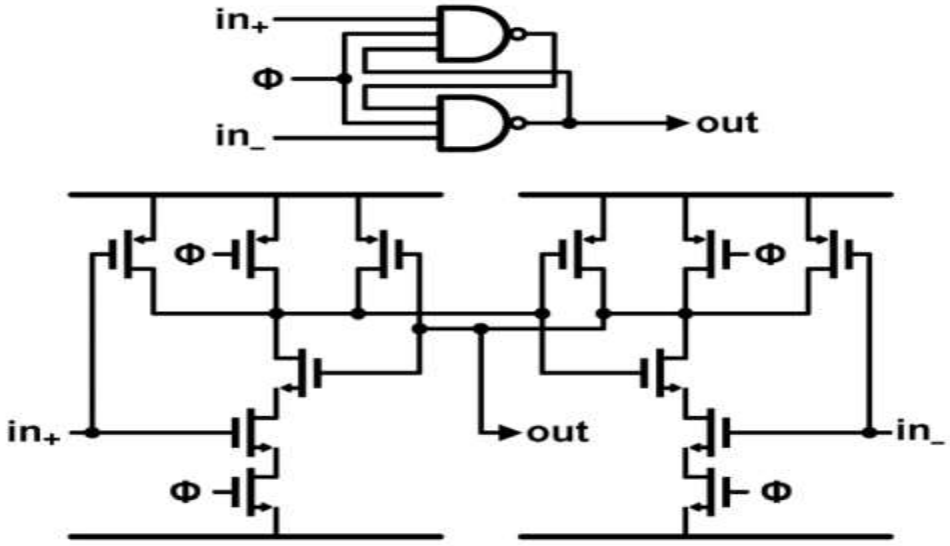

Fig. 6 comparator made from standard digital NAND3 cells.

The comparator operates of of a single phase clock . When the comparator is reset through the parallel PMOS devices. When the discharge through the two series NMOS branches is determined by the differential input. Once the output drops low enough, regeneration occurs, which makes the digital decision. The input common-mode voltage must be high enough to not turn on the PMOS devices connected to the input Upon observation, the schematic of the transistors inside a CMOS NAND3 gate closely resemble half of a clocked analog comparator . By connecting two NAND3 gates together as in Fig, an analog-input comparator is created if the common-mode of the input is high enough to ensure that the PMOS transistors connected to the input are in the cutoff region of operation. When the clock is low, both outputs are reset to the positive supply rail. When the clock goes high, the outputs will begin to discharge through the three series NMOS devices. The discharge rate depends on the capacitance on the output node and the current through the three series devices. Since one of the series devices is connected to the analog input, the discharging current is proportional to the input. Once one of the outputs discharges to below a PMOS threshold voltage, the cross-coupled connection creates positive feedback that causes the comparator to force the outputs all the way to the supply rails. Implementing such a comparator can be done by explicitly referencing the standard library cells in the RTL Verilog code as in Fig. 5(a). In this example, a static SR-latch is added to the output of the comparator. The SR-

latch holds the output data valid while the comparator is reset. The SR-latch input is buffered with inverters to reduce a memory-effect on the comparator due to the SR-latch. Although this circuit is inherently compatible with digital synthesis, the synthesizer will assume that the circuit is actually a digital one, and will try and optimize it by replacing some of the gates or changing the circuit entirely while maintaining the same digital function. This digital optimization may render the circuit nonfunctional from an analog perspective, so here the synthesis directive set_dont_touch comparator, or equivalent, will prevent the synthesizer from altering the comparator module.

```
1  module comparator(INP, INN, CK, Q);
2   output Q;
3   input INP, INN, CK;
4
5   wire op, on, opn, onn, qn;
6   nand3x1 U1 ( .A(op), .B(INP), .C(CK), .Y(on) );
7   nand3x1 U2 ( .A(on), .B(INN), .C(CK), .Y(op) );
8   invx1 U3 ( .A(op), .Y(opn) );
9   invx1 U4 ( .A(on), .Y(onn) );
10  nor2x2 U5 ( .A(qn), .B(opn), .Y(Q) );
11  nor2x2 U6 ( .A(Q), .B(onn), .Y(qn) );
12
13  endmodule
```

(a)

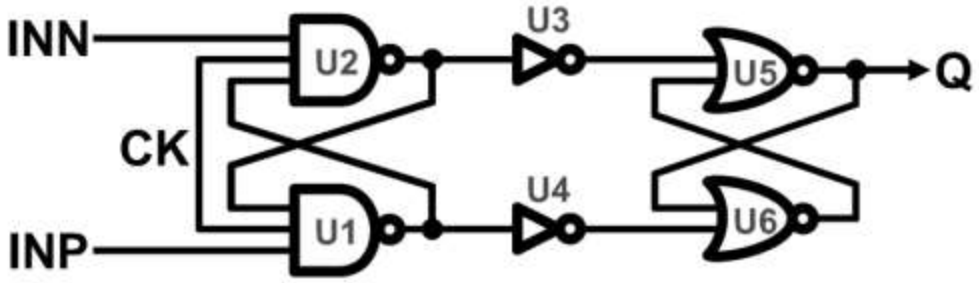

Fig.7 (a) Verilog module ‘comparator’ which implements a NAND3 based comparator (lines 6–11). Inverters buffer the comparator output to a SR-latch. This is to remove any memory effect caused by the latch. (b) Gate-level schematic representation of the code

GDI BASED MUX:

GATE DIFFUSION TECHNIQUE:

The GDI method is based on the use of a simple cell as shown in Fig. At a first glance the basic cell resembles the standard CMOS inverter, but there are some important differences: GDI cell contains three inputs – G (the common gate input of the nMOS and pMOS transistors), P (input to the outer diffusion node of the pMOS transistor) and N (input to the outer diffusion node of the nMOS transistor).

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The Out node (the common diffusion of both transistors) may be used as input or output port, depending on the circuit structure.

The GDI cell is similar to a CMOS inverter structure. In a CMOS inverter the source of the PMOS is connected to VDD and the source of NMOS is grounded. But in a GDI cell this might not necessarily occur. There are some important differences between the two. The three inputs in GDI are namely-
1) G- common inputs to the gate of NMOS and PMOS
2) N- input to the source/drain of NMOS
3) P- input to the source/drain of PMOS

Bulks of both NMOS and PMOS are connected to N or P (respectively), that is it can be arbitrarily biased unlike in CMOS inverter. Moreover, the most important difference between CMOS and GDI is that in GDI N, P and G terminals could be given a supply 'VDD' or can be grounded or can be supplied with input signal depending upon the circuit to be designed and hence effectively minimizing the number of transistors used in case of most logic circuits (eg. AND, OR, XOR, MUX, etc). As the allotment of supply and ground to PMOS and NMOS is not fixed in case of GDI, therefore, problem of low voltage swing arises in case of GDI which is a drawback and hence finds difficulty in case of implementation of analog circuits.

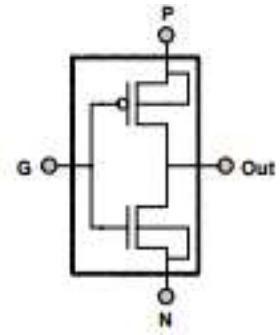

Fig8: Basic GDI cell

Multiple-input gates can be implemented by combining several GDI cells. The buffering constrains, due to possible VT drop are described in detail in [8], as well as the technological compatibility with CMOS (and with SOI). Morgenshtein has proposed basic GDI cell shown in Fig.1 [8]. This is a new approach for designing low powerdigital combinational circuit.GDI technique is basically two transistor implementation of complex logic functions whichprovides in-cell swing restoration under certain operating condition. This approach leads to reduction in power consumption, propagation delay and area of digital circuits is obtained while having low complexity of logic design. Animportant feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of theNMOS is not connected to GND. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design. There are three inputs in a GDI cell - G (common gateinput of NMOS and PMOS), P (input to the source/drain ofPMOS) and N (input to the source/drain of NMOS).Bulks ofboth NMOS and PMOS are connected to N and Prespectively. Table 1 shows different logic functionsimplemented by GDI logic [8] based on different inputvalues. So, various logic functions can be implemented withless power and high speed with GDI technique as comparedto conventional CMOS design.

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S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

RESULTS:

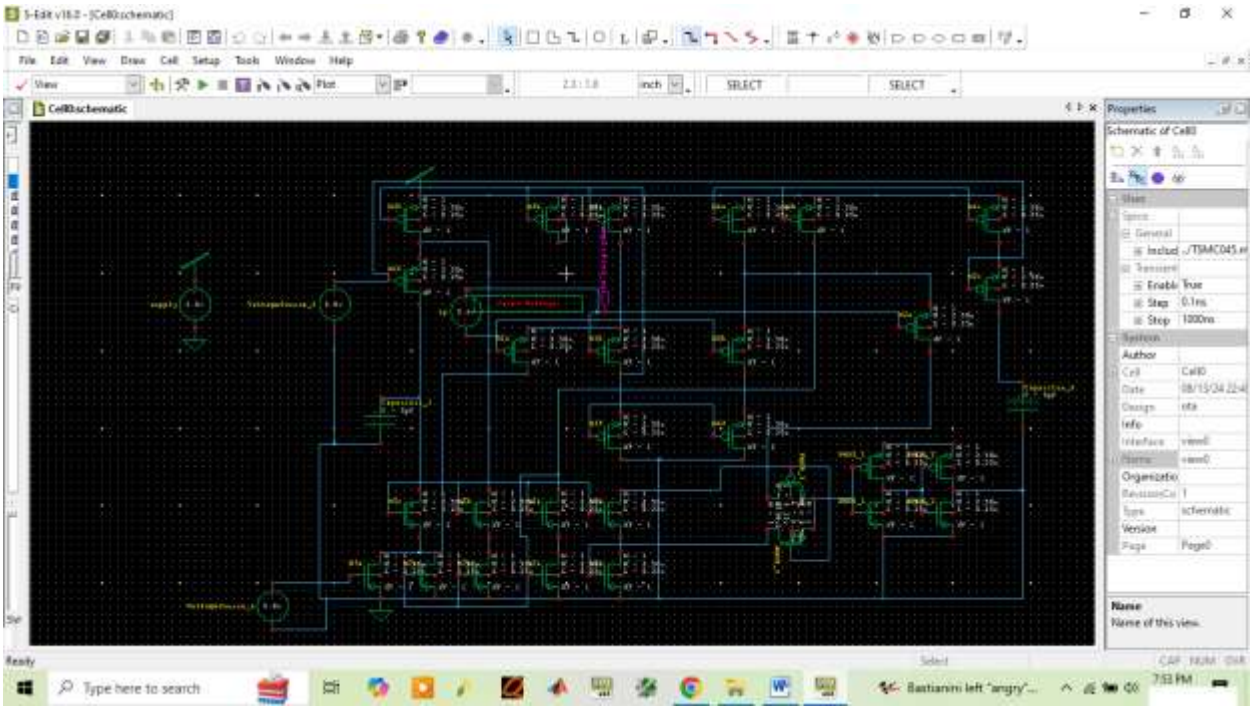

Fig a: Proposed Design in Tanner Tools

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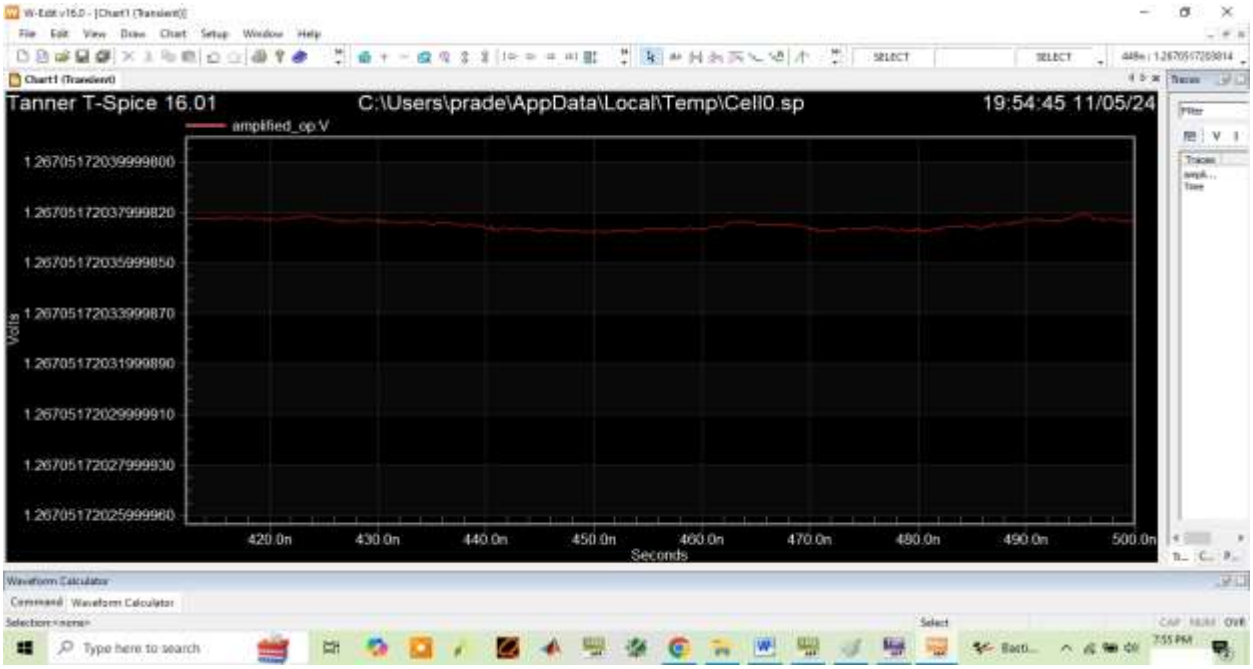

Fig b: Proposed amplified simulation result when input = 0.1V

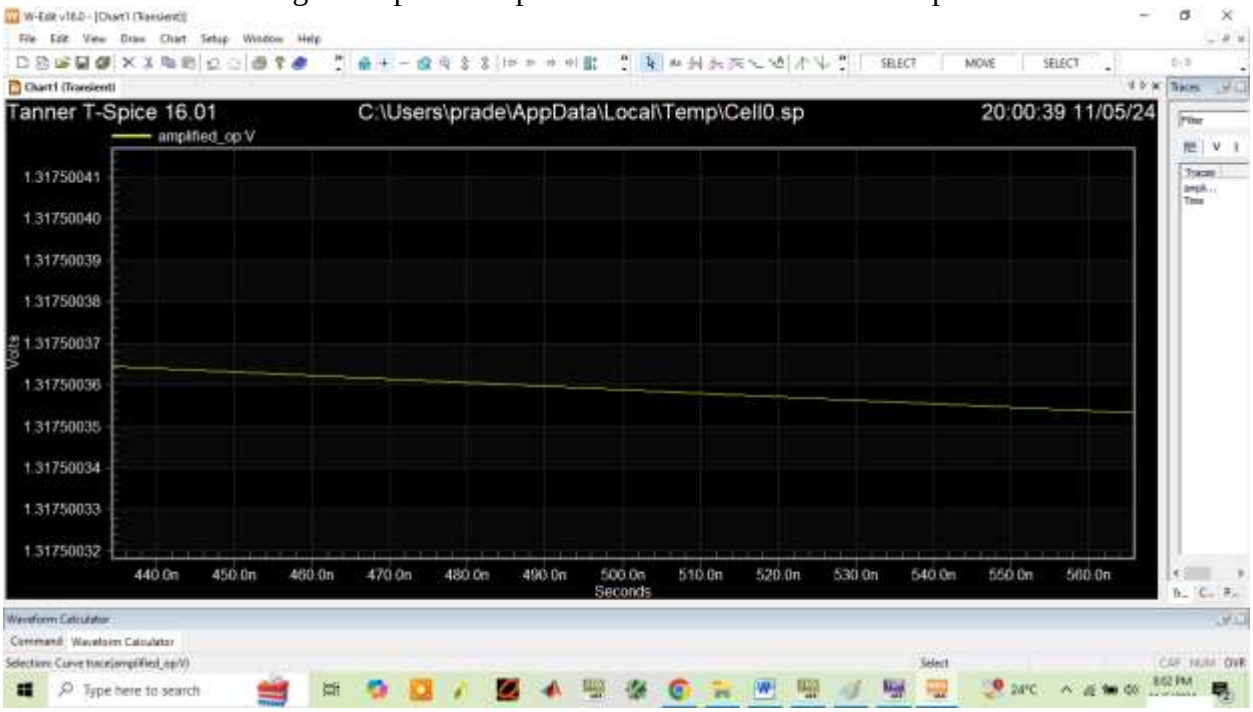

Fig c: Proposed amplified simulation result when input = 0.5 V

CONCLUSION:

Finally, efficient cooperator using fully differential OTA with improved power and area was proposed with GDI based multiplexer. The circuit was fabricated in a 45-nm CMOS process. A comparator that is

implemented as two cross-coupled 3-input NAND gates has been demonstrated to work effectively as a true digital comparator.

FUTURE SCOPE:
By applying low power techniques for the proposed comparator architecture, the static and dynamic power consumption which is the major concern can further be reduced. Critical path delays also can be reduced using sophisticated techniques.

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