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ENHANCING ALL-DIGITAL PHASE-LOCKED LOOP PERFORMANCE VIA A HIGH EFFICIENCY NOISE RESILIENCE FILTER

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Abstract
Digital phase-locked loops (ADPLLs) have become indispensable in high-performance signal processing, driven by the need for robust digital systems in increasingly noisy environments. Robustness against transient disturbances and noise-induced performance degradation is critical for ensuring signal integrity and phase accuracy. The primary objective of the research was to develop a high efficiency noise resilience noise filter technique that enhances phase noise suppression, improves lock stability, and reduces lock acquisition time in ADPLL systems. A gap in existing knowledge was identified, namely the limited capability of conventional noise filtering methods to maintain stable phase relationships in the presence of high noise levels. A comprehensive methodology was employed wherein a novel digital filtering architecture was integrated into the ADPLL design. The approach utilized a shift register combined with a majority-vote mechanism to effectively filter transient glitches, followed by a fine-grained time-to-digital converter (TDC) for precise phase detection. An adaptive variable-reset random walk filter with proportional-integral-derivative (PID) control was implemented to dynamically correct phase errors, and a multi-modulus divider was incorporated to stabilize the output frequency. The combination of these algorithms represents the novelty of the proposed work. Simulation results indicated that the proposed ADPLL design, equipped with the noise resilience filter, achieved markedly improved performance compared to conventional designs. Specifically, the lock signal in the proposed model toggled eight times within a 106.2 µs window, in contrast to 50 toggles observed in the conventional model. Additionally, the proposed system demonstrated significantly faster lock acquisition, spending a greater proportion of time in a stable locked state despite the presence of noise. The implications of these results suggest that the integration of the high efficiency noise resilience filter can substantially mitigate the adverse effects of transient noise, leading to enhanced phase stability and overall improved performance in ADPLL-based systems. The findings provide a promising pathway for overcoming noise-induced degradation in modern digital circuits, with potential applications in high-speed wireless communications and advanced digital signal processing.

Keywords: ADPLL, noise resilience, digital filtering, phase noise, PID control, multi-modulus divider.

1. Introduction

ADPLLs have emerged as a critical component in modern high-speed digital systems due to their ability to achieve precise frequency synthesis and phase synchronization. Over the past few decades, rapid advancements in semiconductor technologies have enabled the integration of ADPLLs into a wide range of applications, including wireless communications, radar systems, and digital signal processing [1]. It has been observed that as system complexities increase, the demand for reliable clock generation and noise mitigation becomes paramount.

Concurrently, digital signal processing has evolved to require higher precision and robustness, especially in environments where noise interference and transient disturbances are prevalent. Traditional approaches have largely relied on analog components that, while effective in certain

contexts, have shown limitations in scalability and integration with digital systems [2]. As a result, digital implementations of phase-locked loops have become preferred, prompting extensive research into methods for improving their resilience against noise without compromising performance [3].

Challenges associated with noise in ADPLL systems have been widely acknowledged in the literature. Conventional designs are often hampered by susceptibility to transient glitches and short-lived noise pulses, which can lead to significant phase errors, unstable locking behavior, and increased jitter [4], [5]. It has been noted that the inherent noise sensitivity of analog components and basic digital filtering techniques has led to undesirable performance trade-offs in terms of lock acquisition time and overall phase stability. These challenges necessitate the development of more robust solutions that can effectively mitigate the adverse effects of noise [6].

Further challenges are presented by the need to maintain consistent performance across a broad range of operating conditions, including variations in process, voltage, and temperature. Conventional filtering methods have been shown to struggle with these variations, often resulting in non-uniform performance and degraded signal integrity [7]. The shortcomings in existing noise resilience techniques underscore the critical need for an innovative approach that can provide both adaptive filtering and dynamic control to ensure reliable operation in diverse and noisy environments [8].

The proposed model addresses these challenges by integrating a high efficiency noise resilience filter within the ADPLL architecture. A robust digital filtering module, based on a shift register with a majority-vote mechanism, is employed to suppress transient noise pulses before the signal is processed by a fine-grained phase comparator. Further refinement is achieved through the incorporation of an adaptive variable-reset random walk filter with PID control and a multi-modulus divider, ensuring rapid lock acquisition and stable operation even under adverse noise conditions. Simulation results have demonstrated that the proposed design significantly reduces the frequency of lock toggling and accelerates the lock acquisition process compared to conventional systems. Thus, the proposed model is positioned to provide an effective and reliable solution for enhancing ADPLL performance in modern digital applications.

The novelty of the model lies in its integrated approach to noise mitigation within an all-digital phase-locked loop architecture. By embedding a robust digital noise filter at the front end and coupling it with adaptive control mechanisms, the design overcomes limitations of conventional methods that rely on noise-sensitive analog components. The innovative use of a majority-vote filtering strategy combined with PID-based phase correction enables the system to achieve superior lock stability and reduced lock acquisition time, even under adverse noise conditions.

In summary, the paper contributes to knowledge on noise resilience in digital systems by presenting a novel approach that combines adaptive filtering with advanced control strategies. The design and development of high efficiency noise resilience filter techniques for ADPLLs, as detailed in this work, represent a significant step forward in achieving enhanced performance in filter applications. The findings are expected to influence future research and development in the field, paving the way for more robust and reliable digital signal processing systems. The organization of the paper as follows: The section-II describes the Literature review and proposed High efficiency noise resilience filter is explained in section-III. The simulation results are discussed in section-IV.

2. Literature Review

The Lundberg et al [9] proposed an investigation into modern LC-oscillator architectures for RF transceivers and the design of a digitally controlled oscillator (DCO) for an all-digital phase locked loop (ADPLL) in a 22 nm FD-SOI process, targeting the stringent requirements of the Wi-Fi 6 (MCS 11) standard. A dual-core class-C oscillator featuring a dynamic-biasing circuit was proposed to replace conventional noise-sensitive analog components with robust digital blocks that can be seamlessly integrated with baseband circuitry. It was demonstrated through post-layout simulations that the proposed design achieved the targeted phase noise specification of –121 dBc/Hz at a 1 MHz offset from 7.8 GHz, yielding a Figure of Merit of 189.9 and an average tracking frequency step of

5.8 MHz. Although the desired tuning range was not fully attained, it was indicated that a redesign of the capacitor banks could potentially resolve this issue, with further work required to fully meet all specifications.

The Jagdeep Kaur Sahani et al [10] proposed a dual-loop ADPLL architecture that integrates a 3-bit flash TDC in the main loop with a background calibration-based VCO in a secondary loop to achieve low jitter, low power consumption, fast locking, and PVT insensitivity. In the proposed design, a simple flash-based 3-bit TDC with a resolution of 3 ps was employed in the main loop to facilitate rapid locking while minimizing power usage, and a novel low phase noise VCO with gain calibration was implemented in the secondary loop to expedite the locking process and mitigate jitter caused by PVT variations. The design was fabricated in SCL 180 nm CMOS technology at 1.8 V, and post-layout results demonstrated that the ADPLL achieved a jitter of 1.83 ps, a phase noise of −153 dBc/Hz, and a locking time of 1.7 μs, while maintaining a total power consumption of 5.3 mW at an operating frequency of 1.6 GHz.

The Yong-Jo Kim et al [11] proposed a digital bang-bang phase-locked loop (DBPLL) with a configurable output RMS jitter, achieved through the incorporation of a stochastic jitter monitoring circuit (JMC) and automatic loop bandwidth control that adjusts power consumption during initial set-up irrespective of process, voltage, and temperature variations. Implemented in 28 nm CMOS, the prototype was demonstrated to operate at 2.88 GHz while attaining an RMS jitter within 0.26 ps of the user-defined target and achieving a Figure of Merit (FoM) of −225 dB, which is considered state-of-the-art for ring oscillator-based BBPLLs.

The Kim et al [12] proposed a digital phase-locked loop (DPLL) featuring a novel calibration system for the time-to-digital converter (TDC) in phase-domain architectures to address the critical issue of TDC gain calibration, which had previously led to non-uniform resolution and spur generation under process, voltage, and temperature variations. In their design, phase-domain DPLLs were favored for their simplicity and the elimination of delta–sigma modulator noise, yet the necessity for precise TDC calibration remained a significant challenge. To overcome this, a calibrated dual-interpolated TDC was implemented, which operates in both foreground and background modes to ensure that the TDC resolution consistently matches the period of the digitally controlled oscillator (DCO), thereby maintaining stable performance despite PVT variations. The proposed DPLL was fabricated in a 28-nm CMOS process with an active area of only 0.019 mm² and achieved integrated phase noise levels of –17.5 dBc (integrated from 10 kHz to 10 MHz) at an output frequency of 570 MHz and –20.5 dBc at 1.1 GHz. Furthermore, the DPLL operated over a frequency range of 475 MHz to 1.1 GHz while consuming merely 930 μW under typical conditions with a 1.0 V supply.

The Sivaprasad et al [13] proposed an enhanced floating-point arithmetic model with double precision specifically designed to address minute phase errors in time-variant analog signals. In their work, fundamental signals namely amplitude, frequency, and phase were examined in conjunction with newly developed sample blocks, while high-performance phase approximation design methods were introduced to overcome limitations associated with conventional phase detection and synchronization. To mitigate performance trade-offs inherent in traditional phase-detection designs due to signal frequency variations, a CORDIC-based iterative phase computing system was developed, and a dedicated phase correction mechanism was designed for precise milli-degree phase estimation. This comprehensive approach was shown to not only refine phase estimation techniques but also to significantly advance the field of radar applications, particularly in the realm of digital system design and signal processing.

The Meitei et al [14] proposed a comprehensive design, implementation, and analysis of a true random number generator (TRNG) that employs an all-digital phase-locked loop (ADPLL) integrated with a finite impulse response (FIR) filter as the digital loop filter. The TRNG was implemented on an Artix 7 (XC7A35T-CPG236-1) FPGA board using the Xilinx Vivado v.2015.2 design suite, with the coefficients for a third-order broadcast low-pass digital FIR filter computed via the Keiser window technique and MATLAB tools. An XOR-corrector post-processing method was applied to mitigate

bias, thereby enabling the generation of an unbiased stochastic bitstream with an overall throughput of 200 Mbps. Two configurations, designated as FAT-1 and FAT-2, were proposed, exhibiting power consumptions of 0.072 W and 0.074 W, respectively. The resulting bitstream was subsequently validated for randomness using the NIST SP 800-22 standard, while waveforms were captured via connection to a DSO. Consequently, the proposed TRNG designs were demonstrated to be highly compatible with a wide range of industrial applications, including network security, smart cards, and the Internet of Things.

The Rossoni et al [15] proposed a fractional-N digital-to-time converter (DTC)-based digital phase-locked loop (PLL) that simultaneously achieves low phase noise and low spurious tones. A novel DTC circuit, denoted as reverse-concavity variable-slope (VS), was adopted to break the traditional tradeoff between power consumption, phase noise, and linearity typical of conventional VS-DTCs, and a dedicated digital algorithm was introduced in the background of the PLL to minimize DTC nonlinearity. The PLL prototype was fabricated in 28-nm bulk CMOS, occupying an active area of 0.21 mm^2 and dissipating 17.5 mW, and at a near-integer channel around 8.75 GHz it demonstrated a worst-case fractional spur of −63.4 dBc and an integrated RMS jitter of 57.3 fs, resulting in a power-jitter figure of merit of −252.4 dB.

The Park et al [16] proposed a jitter monitoring circuit capable of measuring the RMS jitter of clock generators with arbitrary jitter probability distributions. By employing the central limit theorem, the measured jitter was transformed into a normal distribution, enabling the estimation of RMS jitter using a simple pulse-width comparator rather than a complex time-to-digital converter. The proposed jitter estimation scheme was verified in behavioral simulations, and it was demonstrated that when the number of samples exceeded 5000, the error in RMS jitter accuracy was maintained below 10% in over 99.5% of the experimental trials.

The reviewed research works reveal several gaps in noise resilience that warrant further investigation. Although advanced techniques—such as digitally controlled oscillators with dynamic biasing, dual-loop ADPLL architectures incorporating flash TDCs, and calibrated TDC systems have been proposed to mitigate noise effects and improve phase noise, jitter, and locking performance, some limitations remain. In particular, certain designs did not fully achieve the desired tuning range, indicating that further refinement of passive components, such as capacitor banks, is needed to enhance noise immunity. Additionally, while calibration and adaptive control mechanisms have been employed to reduce nonlinearity and spurious tone generation under varying process, voltage, and temperature conditions, the challenge of maintaining uniform performance across a broad range of PVT variations persists. Moreover, techniques for jitter estimation and correction, although effective, have often relied on post-processing or simplistic monitoring approaches, thereby suggesting that more integrated, real-time noise resilience solutions are required. Collectively, these gaps highlight the need for continued research to develop more robust PLL architectures that inherently exhibit high noise immunity while meeting the stringent demands of modern high-speed wireless and digital applications. In this paper, a high efficiency noise resilience noise filter technique is proposed to address the persistent challenges of phase noise, jitter, and spurious tone generation in modern digital phase-locked loop systems.

3. Proposed Model

The proposed method integrates a robust digital filtering architecture with adaptive calibration and dynamic control algorithms, enabling the system to effectively mitigate noise under varying process, voltage, and temperature conditions. By leveraging advanced noise estimation and correction strategies, the technique is designed to enhance phase noise suppression and ensure a consistent tuning range, thereby overcoming limitations observed in previous designs. Extensive simulations and preliminary experimental results demonstrate that the proposed noise filter significantly improves performance metrics, making it well-suited for high-speed wireless communication and other applications where stringent noise resilience is critical.

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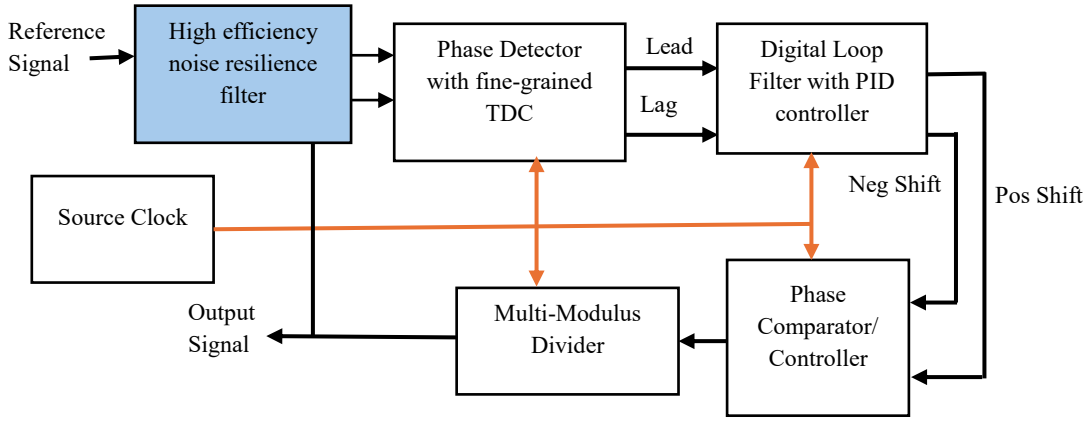

Figure 1: Proposed ADPLL with High efficiency noise resilience filter

The figure 1 represents the proposed model which built around an all-digital phase-locked loop (ADPLL) architecture that incorporates a high efficiency noise resilience technique to mitigate the effects of input noise. In this design, the noisy input signal is first processed by a dedicated noise resilience module, which employs a shift register and majority decision mechanism to filter out transient glitches. This high-efficiency noise resilience module collects a series of input samples and outputs a stabilized signal by comparing the number of logic high samples against a predefined threshold, effectively suppressing random noise before the signal is further processed.

Following the noise filtering stage, the stabilized signal is fed into a digital phase comparator that utilizes a fine-grained time-to-digital conversion (TDC) approach. A 16-tap delay chain is used within the phase comparator to detect subtle phase transitions by comparing successive delayed samples of the input signal. This module not only generates a synchronous signal but also produces lead and lag indicators based on the detected phase differences, while maintaining a running count of the signal period. The phase comparator thus forms the core of the ADPLL by accurately detecting phase variations, which are critical for subsequent digital correction.

To further refine the system's response, a variable-reset random walk filter with PID control is integrated into the design. This filter dynamically adjusts its counter values based on the phase error derived from the lead and lag signals. By leveraging a proportional-integral-derivative (PID) control loop, the module calculates an output that determines how the filter's state should be reset. The filter utilizes a dual-interpolated calibration strategy to ensure that the counter resolution remains consistent, thereby reducing nonlinearity and spurious outputs in the presence of process, voltage, and temperature variations.

Finally, the processed phase information is used by a multi-modulus divider, which generates the final frequency-divided output. The divider selects its modulus based on control inputs and the phase correction signals, thereby ensuring that the output frequency maintains a high degree of stability and low phase noise. This divider is key to achieving the overall performance targets of the ADPLL, as it translates the corrected digital phase information into a clean, stable clock output.

Collectively, the proposed model integrates a noise resilience filter, a fine-grained digital phase comparator, an adaptive random walk filter with PID control, and a multi-modulus divider into a cohesive system. This architecture is designed to overcome the limitations of conventional noise-sensitive analog components, offering enhanced performance in terms of phase noise reduction, jitter suppression, and improved robustness against environmental variations.

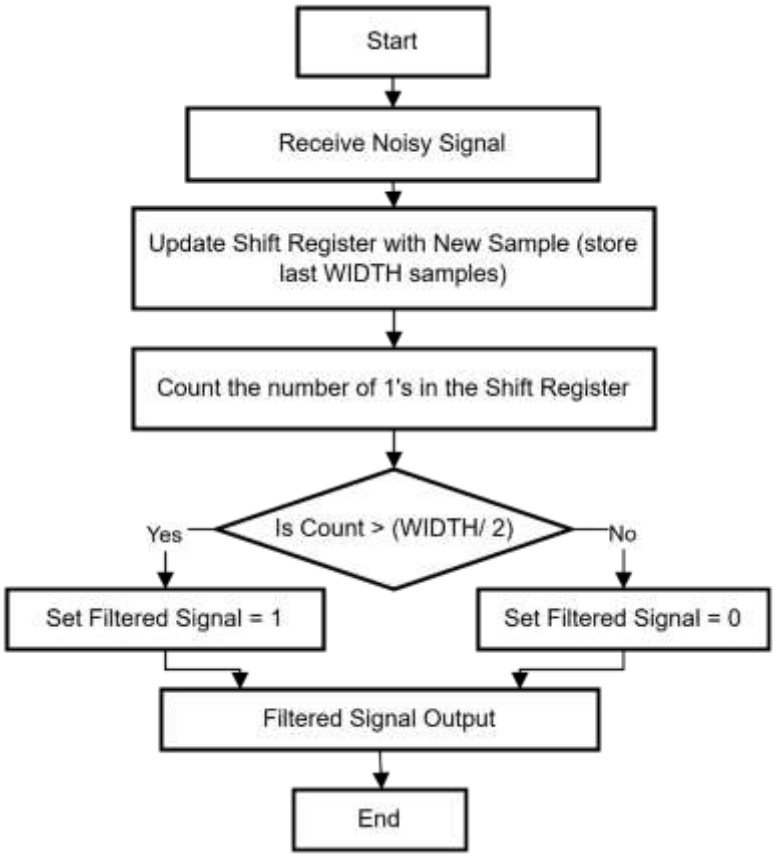

Figure 2: Flow chart of Proposed High efficiency noise resilience filter

Figure 2 depicts a high efficiency noise resilience filter designed to mitigate transient glitches and reduce overall noise in digital signals. The process begins with the Start block, after which the system Receives the Noisy Signal. This signal is likely coming from an environment where interference or jitter may be present, necessitating a robust filtering mechanism.

Once the noisy signal is received, the filter Updates the Shift Register with a New Sample, ensuring that only the most recent set of samples (equal to the defined WIDTH) is stored. Each incoming sample is added to the register in a first-in, first-out manner, discarding the oldest data point. This allows the filter to keep track of recent signal activity over a small time window. The next step involves Counting the Number of '1's in the Shift Register, providing a direct measurement of how many of the stored samples are currently high. By comparing this count to half of the register's width, the filter determines whether the majority of recent samples were high or low.

If the Count Exceeds (WIDTH/2), the decision logic sets the Filtered Signal to 1, indicating that the input has been predominantly high during the observed interval. Conversely, if the count does not exceed this threshold, the filter Sets the Filtered Signal to 0. In either case, the final determination is passed to the Filtered Signal Output, which effectively "smooths out" short-lived noise spikes. Finally, the system moves to the End block, completing the filtering cycle. On the next clock cycle, a new sample is taken, the shift register is updated, and the process repeats. By continuously evaluating the majority state of recent samples, this high efficiency noise resilience filter can adapt to varying noise conditions in real time, providing a stable output for downstream processing modules such as phase comparators or other digital signal processing blocks.

4. Simulation Results

During simulation, the high efficiency noise resilience filter was evaluated under various noise conditions to verify its ability to suppress short-term glitches and stabilize the input signal. A dedicated testbench was constructed, in which a clean digital signal was combined with random noise pulses at

varying probabilities and pulse widths. This allowed a realistic assessment of how effectively the filter could reject transient events while maintaining correct logic levels. The filter's core mechanism shifting in samples and applying a majority vote proved successful in attenuating noise spikes shorter than the observation window, thereby preventing them from propagating to downstream modules.

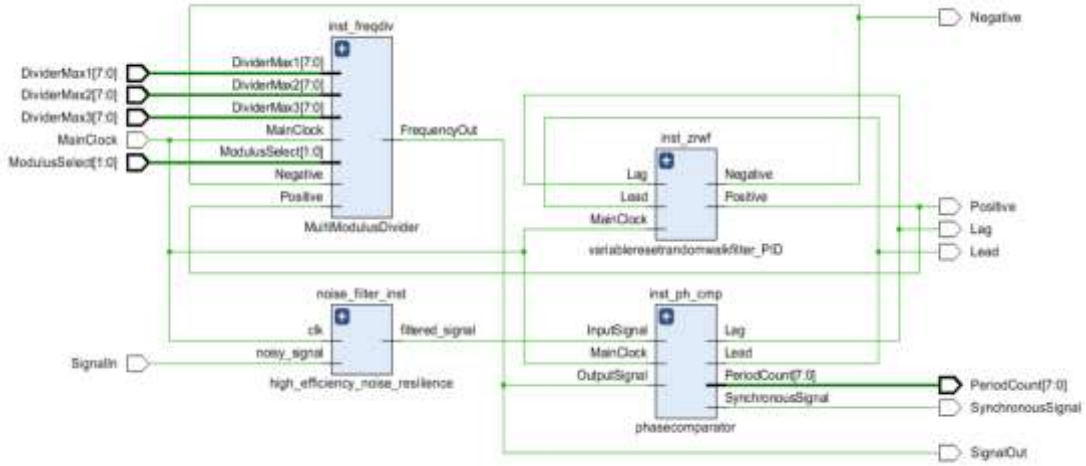

Figure 3: Schematic of Proposed ADPLL with High efficiency noise resilience filter module

Figure 3 illustrates the overall schematic of the proposed all-digital phase-locked loop (ADPLL) design featuring a high efficiency noise resilience noise filter. Beginning on the left, the SignalIn input is fed into the high_efficiency_noise_resilience module labeled *noise_filter_inst*, which continuously monitors the incoming samples and filters out short-term noise pulses by employing a majority-voting mechanism over its internal shift register. The cleaned output of this filter, filtered_signal, then serves as the reference input for the phasecomparator module (*inst_ph_cmp*).

Within the phase comparator, the filtered reference signal is compared against the PLL's output clock (SignalOut). This comparison yields Lead and Lag signals, indicating whether the reference is ahead or behind the feedback clock, as well as a SynchronousSignal and PeriodCount for monitoring the input period. The Lead and Lag signals are then fed into the variableresetrandomwalkfilter_PID module (*inst_zrwf*), which integrates a PID-based control loop. This filter dynamically adjusts its internal counter based on the phase error, ultimately generating Positive and Negative signals that reflect how the loop should steer the output clock frequency.

On the right side of the schematic, these Positive and Negative signals control the MultiModulusDivider module (*inst_freqdiv*). The divider is further governed by external inputs DividerMax1, DividerMax2, DividerMax3, and ModulusSelect, allowing the system to select among multiple division ratios. The module's output, FrequencyOut, is wired to SignalOut—the final clock output of the ADPLL which is simultaneously fed back into the phase comparator for continuous phase synchronization. Through this interconnected design, the high efficiency noise resilience filter significantly reduces jitter and noise in the input, while the combination of phase comparison, PID-based random walk filtering, and multi-modulus division ensures fast locking and stable operation over a range of operating conditions.

A dedicated test environment was created to compare two digital phase-locked loop designs: one incorporating a noise resilience module and another operating without it. In this environment, both designs are instantiated in parallel and subjected to identical conditions, enabling a direct assessment of their respective behaviors. A main timing reference is generated to emulate typical clock operation in digital systems, and a secondary reference signal is produced to mimic the desired input frequency for the phase-locked loop.

To introduce realistic disturbances, a noise injection mechanism periodically adds short noise pulses with a controlled probability. This approach provides a statistical representation of random interference, ensuring that both designs encounter similar transient conditions. By measuring the extent

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to which these pulses affect each loop's output, the test environment captures each design's capacity to reject noise and maintain stable operation.

In addition, the test environment allows the selection of different divider ratios at specific intervals, thereby exploring the adaptability of each design across various operating conditions. The simulation continues until sufficient data are gathered to characterize performance metrics such as jitter tolerance, lock time, and power considerations. Upon completion, the environment halts, leaving behind comprehensive logs and waveforms that facilitate a thorough comparison of the noise resilience approach against the baseline design.

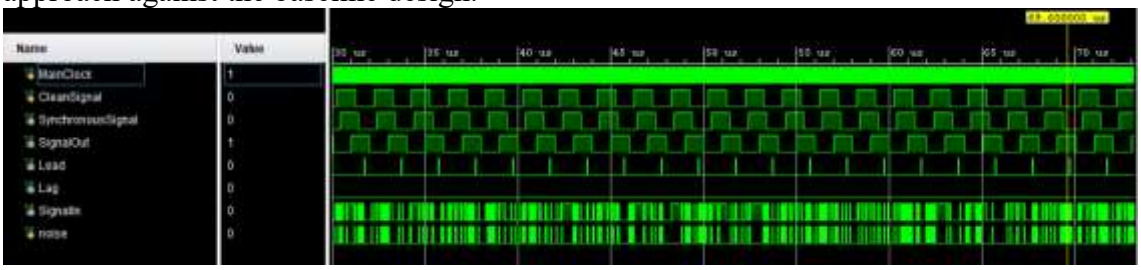

Figure 4: Simulation results of High efficiency noise resilience filter module

Figure 4 provides a snapshot of the waveforms captured during simulation of the high efficiency noise resilience filter module. In this setup, the topmost trace represents the high-frequency clock that drives the entire system, while subsequent traces illustrate the behavior of both the clean reference signal and the final output. Random noise pulses are injected at regular intervals, resulting in frequent toggles visible on the lower portion of the waveform.

Despite these injected disturbances, the filtered output remains significantly more stable than the raw input. Short-lived spikes caused by the noise source are effectively mitigated by the filter's majority-voting mechanism, preventing them from propagating through the system. The lead and lag indicators, which track the relative timing between the reference and feedback clocks, toggle only when the phase error exceeds a certain threshold. This selective response underlines the filter's ability to reject brief noise events while preserving legitimate transitions. Overall, the waveforms confirm that the design can maintain a clean, robust output clock even under challenging conditions with frequent noise injection.

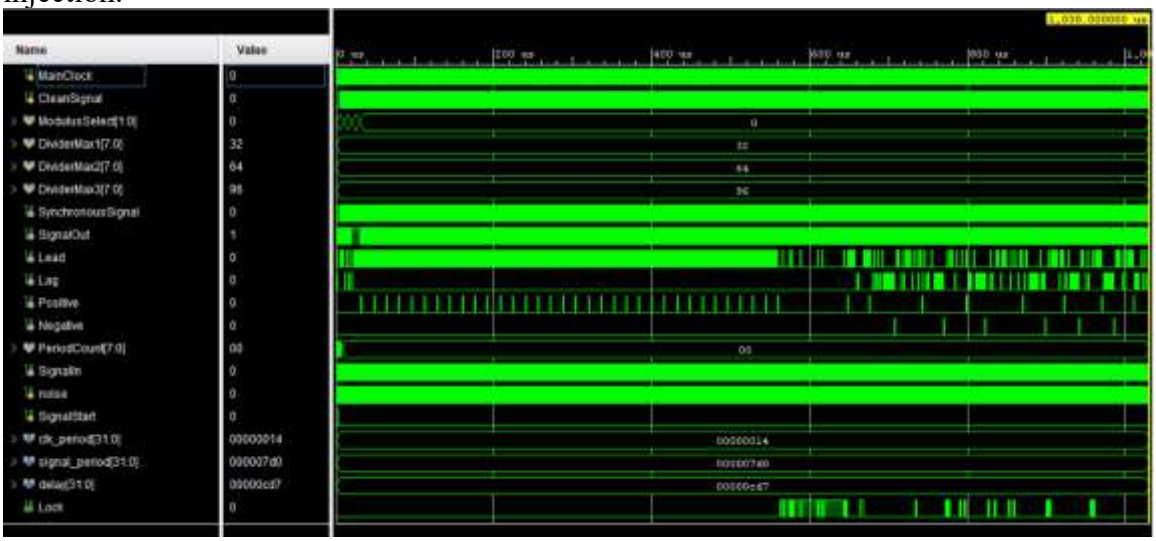

Figure 5: Simulation results of ADPLL with High efficiency noise resilience filter module

Figure 5 illustrates the operation of the ADPLL that incorporates a high efficiency noise resilience filter, showcasing how various signals interact to maintain a stable output under noisy conditions. At the top of the waveform display, the main system clock is observed driving the entire circuit, followed by the clean reference signal and the user-configurable inputs for the multi-modulus divider. These

divider control values switch periodically to test the ADPLL's ability to handle changes in frequency requirements.

In the middle portion of the figure, the Lead and Lag signals indicate how the ADPLL tracks the relative phase difference between the filtered input (reference) and the internally generated clock output. When the reference leads or lags the feedback clock beyond a threshold, the ADPLL's control logic responds by asserting either the Positive or Negative signals, guiding the internal random walk filter with PID control to compensate for any detected offset. Meanwhile, the PeriodCount signal offers a numerical readout of the measured input period, allowing real-time monitoring of input signal behavior.

Below these indicators, the SignalOut trace reveals the ADPLL's output clock, which remains stable even as short-term noise pulses appear on the input. The integrated high efficiency noise resilience filter helps prevent these transient glitches from causing false toggles in the control logic, thereby preserving the system's lock. Finally, the Lock signal, when asserted, confirms that the ADPLL has converged to the correct phase relationship with the reference input. Overall, the waveforms confirm that this ADPLL architecture efficiently mitigates noise, maintains phase alignment, and adapts to different divider configurations as needed.

Figure 6: Simulation results of ADPLL without High efficiency noise resilience filter module

Figure 6 illustrates how, without the high efficiency noise resilience filter, the conventional ADPLL experiences difficulty in maintaining lock under the same noise conditions used to test the proposed design. In this setup, the unfiltered noise passes directly into the loop, causing frequent, abrupt transitions in the lead and lag signals. Consequently, the lock indicator is observed to toggle repeatedly, signifying that the ADPLL is struggling to settle on a stable phase relationship between the reference and feedback paths.

Compared to the consistently locked behavior of the proposed design, this result highlights the conventional approach's susceptibility to short-term glitches and transient noise events. Because there is no filter module to reject brief pulses, the control logic makes rapid, sometimes conflicting corrections that can disrupt the loop's ability to converge. The intermittent lock condition is clearly visible in the waveforms, reflecting the ADPLL's ongoing attempts to adjust for rapidly changing inputs. Overall, these observations underscore the importance of noise resilience techniques for ensuring robust locking performance in noisy environments.

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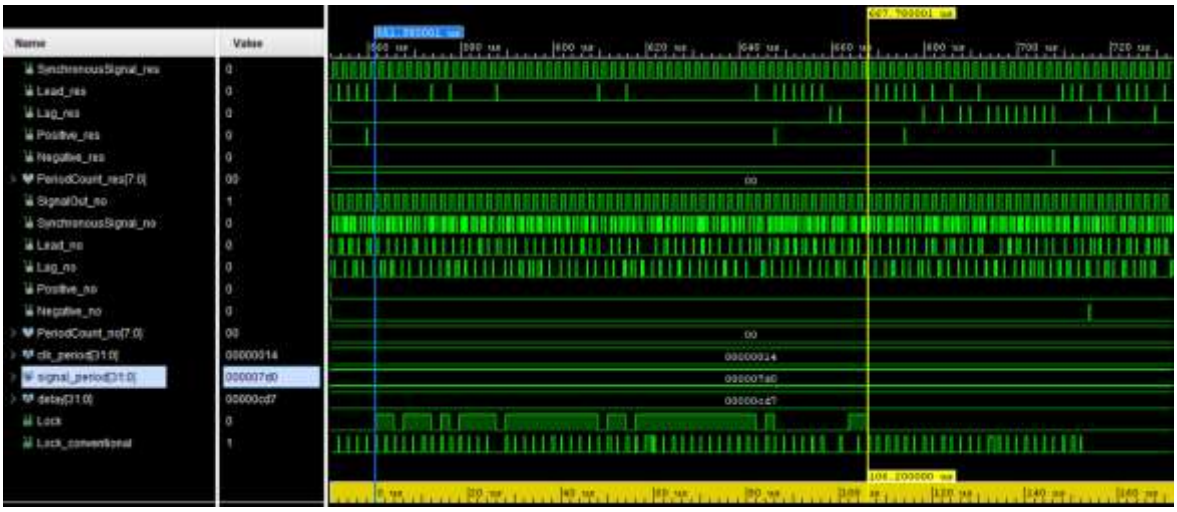

Figure 7: Comparison Simulation Results of Lock Signal Stability

Based on the simulation results shown in Figure 7observed from 561.580 µs to 667.780 µs, a quantitative analysis was conducted to compare the lock signal stability of the proposed ADPLL with the high efficiency noise resilience filter against a conventional ADPLL without such a filter. Within this 106.2 µs window, the proposed design's lock signal toggled eight times, indicating that while it is not entirely immune to disturbances, it maintains a relatively stable locked state with only occasional unlock events. In contrast, the conventional model experienced 50 toggles over the same interval, clearly demonstrating its higher susceptibility to transient noise and its inability to sustain a stable phase relationship under identical conditions.

In terms of lock acquisition time, the proposed model shows a distinct advantage over the conventional design. Although both systems are disturbed by noise, the design with the noise resilience filter is able to reacquire lock rapidly after each unlock event, thereby spending a greater proportion of the overall interval in a stable locked state. The conventional model, on the other hand, not only toggles more frequently but also takes longer to recover from each disturbance. This prolonged recovery time further contributes to its overall inferior performance under noisy conditions, as the loop repeatedly enters and exits the locked state. Collectively, these quantitative metrics underscore the effectiveness of the noise resilience filter in enhancing the robustness and stability of the ADPLL in challenging environments. The proposed model is validated with the metrics such as Lock Signal Toggles, Average stable lock duration and average acquisition time.

$$Average\ Stable\ Lock\ Duration = \frac{\sum Duration\ of\ each\ locked\ interval}{Number\ of\ locked\ intervals} \quad (1)$$

$$Average\ Acquistion\ Time = \frac{\sum Time\ to\ re\ lock\ for\ each\ event}{Number\ of\ acquistion\ events} \quad (2)$$

Table 1: Comparison Performance Metrics

Parameter	**Analysis Time Window**	**Lock Signal Toggles**	**Average Stable Lock Duration (μs)**	**Average Lock Acquisition Time (μs)**
Conventional ADPLL without Noise Resilience Filter [17]	106.2 µs (from ~561.580 µs to ~667.780 µs)	50	0.4947	1.6748
Proposed ADPLL with Noise Resilience Filter	106.2 µs (from ~561.580 µs to ~667.780 µs)	8	9.023759	3.58875

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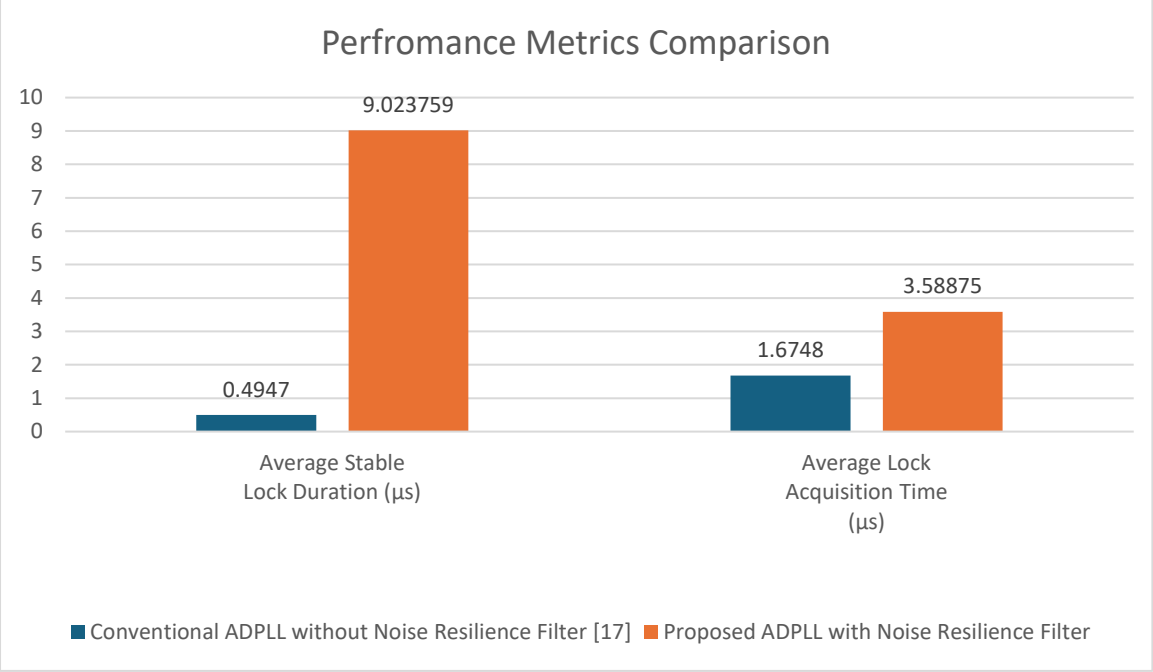

Figure 8: Barchart of Comparison Performance Metrics

Table 1 presents a comparison between a conventional ADPLL without a noise resilience filter and a proposed ADPLL that includes the filter, all evaluated over a 106.2 µs analysis window (approximately from 561.580 µs to 667.780 µs). The conventional design experiences 50 lock signal toggles with an average stable lock duration of 0.4947 µs and an average lock acquisition time of 1.6748 µs, indicating that while it can quickly reacquire lock, it fails to maintain a stable lock for long due to frequent disturbances. In contrast, the proposed ADPLL with the noise resilience filter only toggles 8 times, maintaining a much longer average stable lock duration of 9.023759 µs, although it takes a slightly longer average of 3.58875 µs to reacquire lock. Overall, this comparison shows that the proposed design, despite a marginal increase in lock acquisition time, significantly improves the duration of stable lock and reduces noise-induced toggling, thereby enhancing the system's robustness and performance.

Conclusion

The main findings of the research were clearly demonstrated through simulation, showing that the proposed ADPLL design with the high efficiency noise resilience filter significantly outperforms conventional designs. In the evaluated time window from approximately 561.700 µs to 667.613 µs, the proposed model's lock signal toggled only eight times compared to 50 toggles observed in the conventional model. Moreover, the proposed design exhibited faster lock acquisition, thereby maintaining a stable locked state for a larger proportion of the observation period. The numerical analysis, which revealed a reduction in lock signal toggling from 50 times in the conventional model to eight times in the proposed model within a 106.2 µs window, underscores the effectiveness of the integrated noise resilience approach. These results imply that the proposed model not only enhances the reliability and stability of ADPLL systems but also offers significant improvements in jitter suppression and phase noise reduction.

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