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DATA RETENTION TCAM ARCHITECTURE WITH SLEEPY KEEPER APPROACH

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ABSTRACT
The Ternary Content Addressable memory (TCAM) and Data Retention-based TCAM (DR-TCAM) are Widely used in the routing tables due to its high lookup performance. However, a large number of transistors would cause the power consumption in both designs. In this brief, we propose a novel design to address the inefficiencies of DR-TCAM. Our approach, named the "DATA RETENTION TCAM (DR- TCAM) ARCHITECTURE WITH SLEEPY KEEPER APPROACH" aims to reduce Power Consumption. By dynamically adjusting the power for mask cells based on data features, our design achieves the significant improvements. Based on TSMC 50nm technology, the simulation results shows that the DR- TCAM Architecture with sleepy keeper Approach performs better than the TCAM and DR-TCAM works.

Index Terms –
TCAM , DR-TCAM, Mask Cells, Sleepy Keeper Approach.

INTRODUCTION
Mobile communication is essential in today's world, powering various applications like video streaming, online gaming, and navigation. To meet the demands of these applications, networks need to provide fast communication with minimal delays, high speed, and efficient data routing. Traditional routers face challenges in achieving these requirements, but ternary content addressable memory (TCAM) offers a solution. TCAM enables rapid data searches and efficient routing, but its use can lead to increased power consumption due to the large number of transistors involved.
To decrease TCAM's power consumption when it's not actively used, several methods have been proposed over the past decade [1]-[6]. Including the Data Retention-Based Low Leakage Power TCAM for Network Packet Routing[1] , which leverages data retention principles to minimize power leakage efficiently. Additionally, optimizing the SRAM structure[2], employing a dual-voltage architecture[3], and utilizing dynamic power sources[4]. While these techniques effectively reduce TCAM's power consumption, they may result in data loss if the power supply or data signals are interrupted. To recover lost data, external storage or control signals are needed, which can increase both power usage and data recovery time.
In this brief, a novel DR-TCAM architecture with Sleepy Keeper Approach is proposed to reduce the power consumption of DR-TCAM. Implementing the sleepy keeper approach in our design introduces a dynamic power management technique that efficiently minimizes power consumption. By employing a switch controlled by both a sleep PMOS and sleep NMOS, we can effectively regulate power usage during idle or low activity periods. This strategy optimizes energy utilization by selectively activating and deactivating components, thereby reducing unnecessary power drain. The sleepy keeper method not only enhances overall power efficiency but also prolongs the battery life of our device.

LITERATURE SURVEY
In this Literature Survey, we discusses various techniques proposed for reducing power consumption in Ternary Content Addressable Memory (TCAM) used in network packet routing. We specifically review the most IEEE papers on the subject.
[1]Chang et al. (2021) introduce the Data Retention-based TCAM (DR-TCAM) technique, which exploits the continuity of mask data to enhance power efficiency, particularly in the context of 40nm technology. Building on this, [2] Chen et al. (2016) propose a Filter-Based Dual-Voltage Architecture

designed to reduce power consumption in TCAM, leveraging advancements in 40nm fabrication processes.

Further, [3] Chang (2010) presents the Dynamic Power Source (DPS) methodology, wherein TCAM power usage is minimized through the integration of prefix power source with mask data. However, this approach raises concerns about the stability of TCAM cells, particularly noticeable in 45nm technology. In a different vein, [4] Chang et al. (2013) suggest a Low Leakage TCAM design employing Two-Side Self- Gating, which segments mask cells to effectively diminish power consumption, especially in the realm of 90nm technology.

EXISTING DESIGN

The Traditional TCAM architecture & Data retention based TCAM (DR-TCAM) represent the existing Designs.

1. Traditional TCAM Architecture

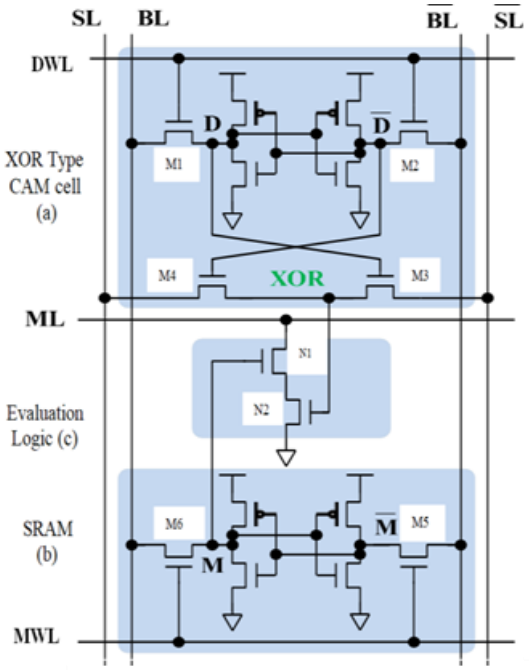

Fig.1 One Traditional TCAM

M	D	S	State	ML	
0	0	0	0	H	Normal-Match
0	1	1	1	H	Normal-Match
0	0	1	0	L	Mismatch
0	1	0	1	L	Mismatch
1	0	0	X	H	Wild Match
1	1	1	X	H	Wild Match
1	0	1	X	H	Wild Match
1	1	0	X	H	Wild Match

The core of TCAM is an array of TCAM cells. AS shown in fig.1 typical TCAM cell consists of three major components. (1) The first component is an XOR-type CAM cell that not only stores the actual data, but also compares the stored data with the searched data. (2) The second component is the mask cell, which is SRAM cell used to store the mask bit to indicate whether this TCAM is in the don't care (X) state or not.

(3) The third component is the evaluation logic to either pull down the ML or not.

As shown in Fig.1(a), this can be simply implemented with two NMOS transistors placed in serial, which are controlled by the mask bit and the XOR result of CAM cell, respectively. In, since the conventional TCAM use the differential SL and differential bit line schemes to perform the search and

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read/write operations, each TCAM column contains two SLs(SL,) and two bit lines(BL,). In the horizontal dimension, besides the ML, each TCAM row also contains the data word line (DWL) and the mask word line (MWL) to write the data and mask bit individually. Clearly, the TCAM is very costly in both the transistor count and the interconnection wire. The most distinct feature of the TCAM cell is that it has three states, i.e., "0,", "1," and "don't care" (or "X") states.

As shown in Fig. the TCAM state is determined by the mask bit and the stored data. In this paper, the mask bit means that this TCAM cell is set to the "X" state, in which there is always a match regardless of the comparison result of the CAM cell. Such comparison is referred to as wild match. In contrast, if the mask bit is 0, this TCAM cell is in either "0" or "1" state, depending on the stored data. In case of, if the search data are equal to the stored data.

2. Data Retention-based TCAM (DR-TCAM)

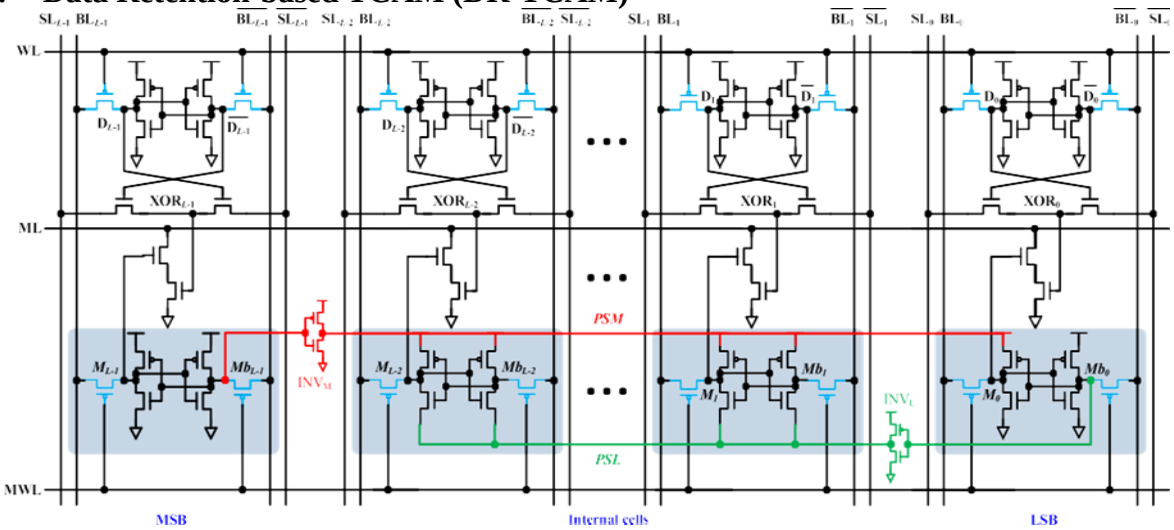

Fig.2: The low leakage TCAM design with data retention technique

In the DR-TCAM design, each TCAM entry is partitioned into several segments. In each segment, the power source of internal mask cells drives from the most significant bit (MSB) and least Significant Bit (LSB) cells, respectively. Due to the continuous feature of mask data, except for the boundary segment, all segments would be inactivated to minimize the leakage power consumption.

Fig.2 shows one DR-TCAM segment, in which two inverters, i.e., INVM and INVL, are inserted to provide Vdd(Charge) path and Gnd (discharge) path for the SRAM cells. The Vdd of internal mask cells comes from the MSB cell, and all the GND of internal mask cells comes from the LSB cell. Note that the Vdd of leftside inverter of the LSB cell is also connected with PSM to lower the leakage currents of the LSB cell in all 0s segment. Since the leakage currents of NMOS is larger than that of PMOS with the same feature size. To further reduce the leakage power consumption, instead of using NMOS, the pass transistors of CAM and SRAM cells are replaced by PMOS.

PROPOSED DESIGN

The proposed design combines a "Data Retention-based TCAM (DR-TCAM) with Sleepy Keeper Approach" to minimizes the power Consumption effectively while ensuring critical data preservation. Similar to the Sleepy Keeper, transistors gating Vdd and Gnd are integrated into the DR-TCAM design. These transistors referred to as sleep transistors, are activated by Sleep signal(SKP) and sleep signal Bar(SKN).When the Logic circuit is in Sleep mode, these sleep transistors disconnect the circuit from both Vdd and Gnd, effectively cutting off power supply to the circuit during idle periods, reducing power consumption. This integration optimizes Power management and safeguards important data, even in the absence of Power.

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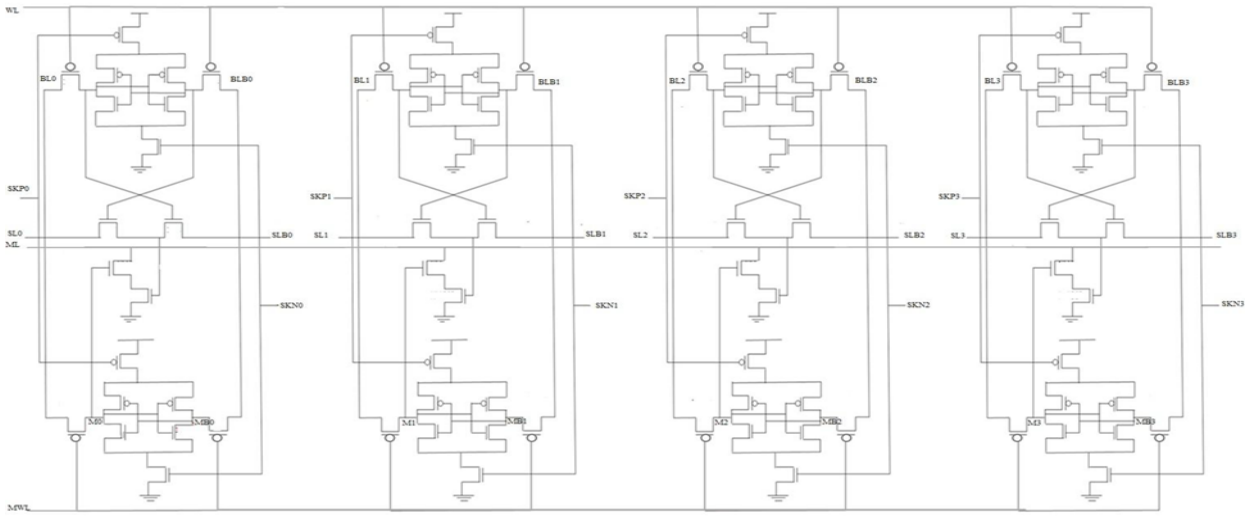

Fig.3: Proposed Design of DR-TCAM with Sleepy Keeper

RESULT ANALYSIS

Traditional TCAM

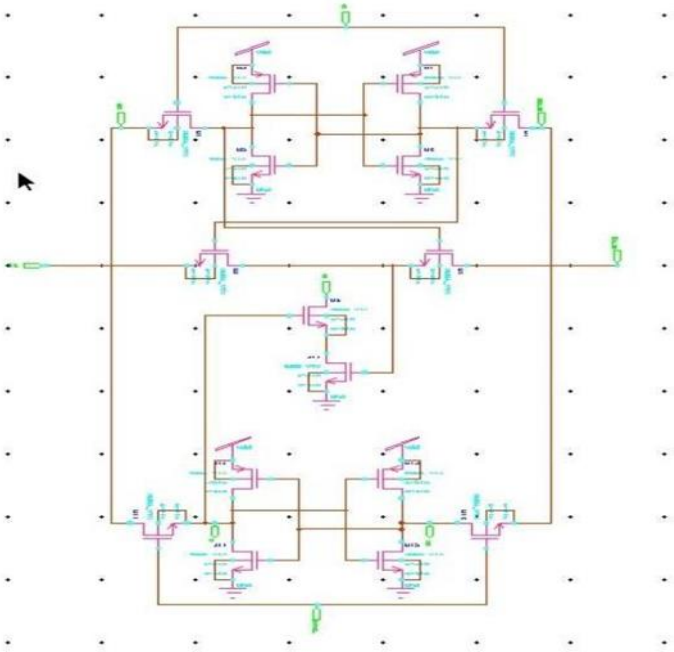

Fig.4 Schematic of Traditional TCAM

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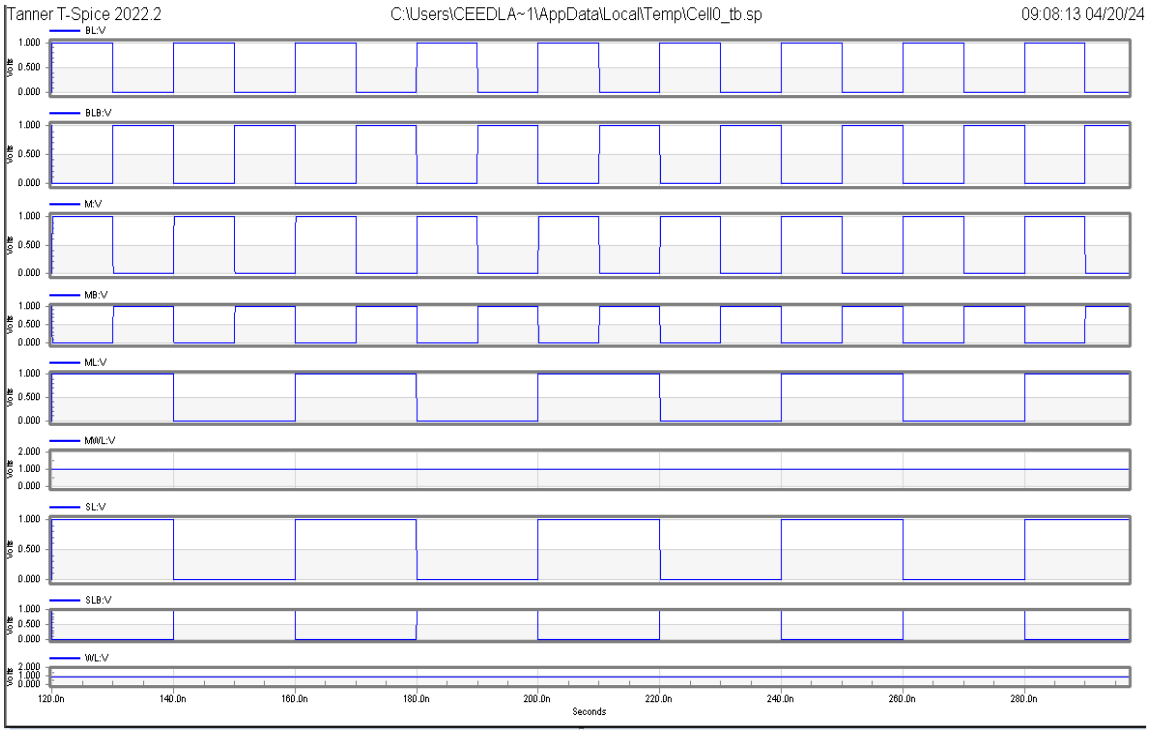

Fig.5 Waveforms of Traditional TCAM

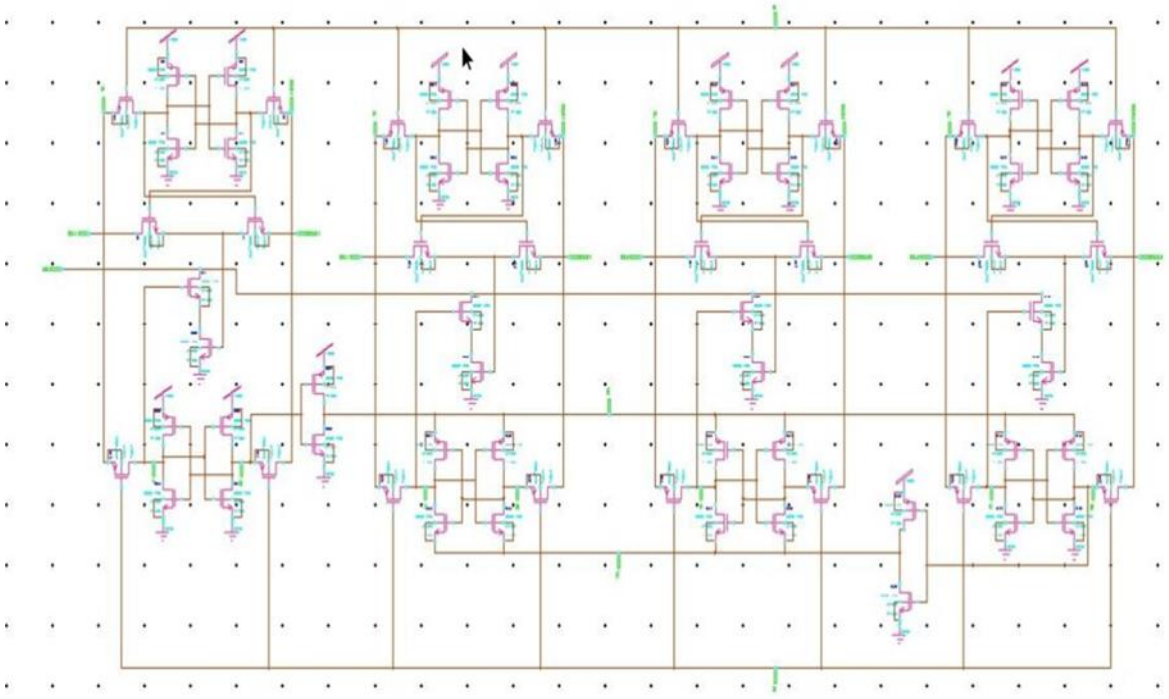

Fig.6 Schematic of Data Retention TCAM (DR-TCAM)

Data Retention TCAM (DR-TCAM)

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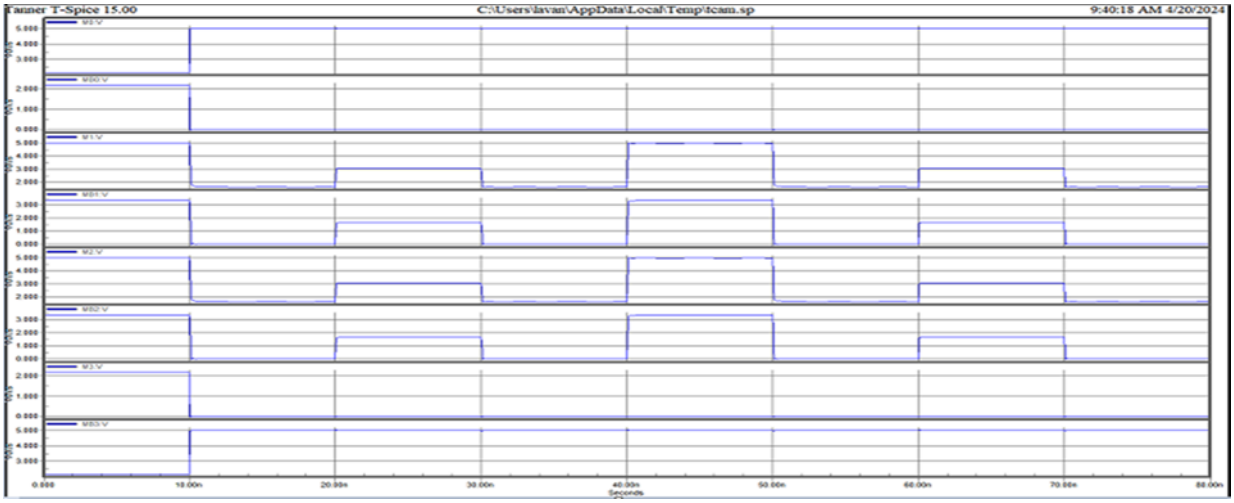

Fig.7 Waveforms of Data Retention TCAM (DR-TCAM)

Data Retention TCAM (DR-TCAM) with Sleepy Keeper Approach

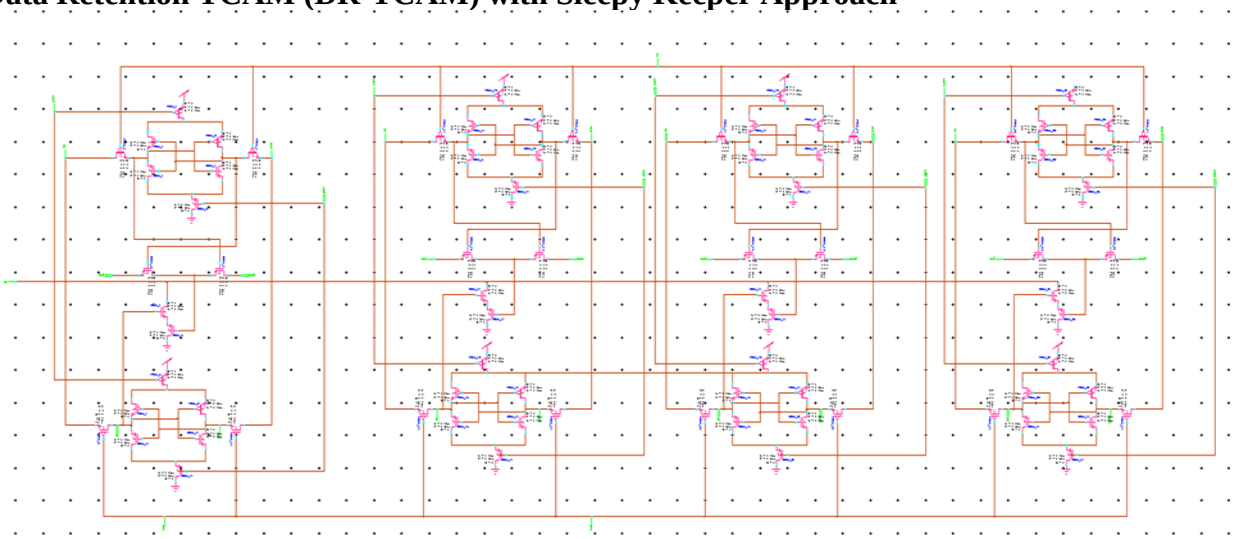

Fig.8 Schematic of Data Retention TCAM (DR-TCAM) with Sleepy Keeper Approach

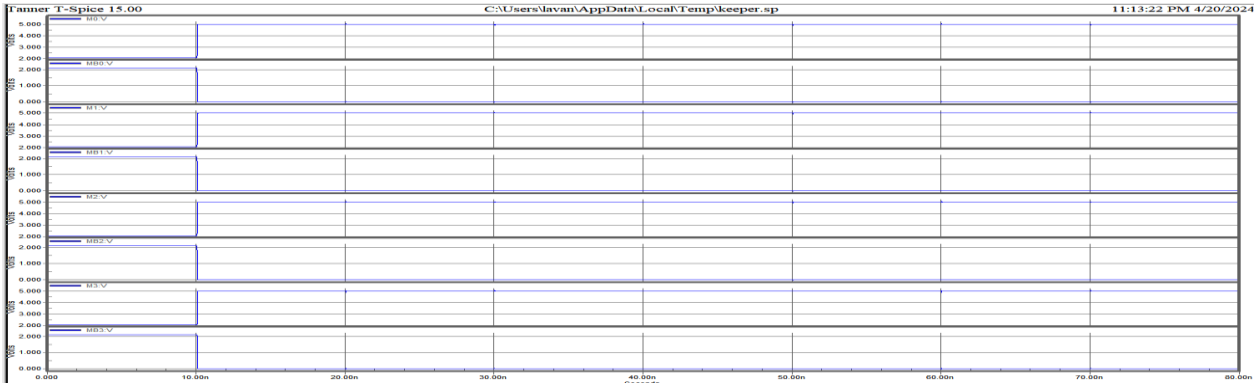

Fig.9 Waveforms of Data Retention TCAM (DR-TCAM) with Sleepy Keeper Approach

Tabular Calculations

	No. of. Transistors	Power(nw)	Delay(ns)
TCAM	16	0.529nw	19.9795ns
DR-TCAM	68	0.156nw	19.906ns
DR-TCAM with Sleepy Keeper Approach	80	0.026nw	9.2743ns

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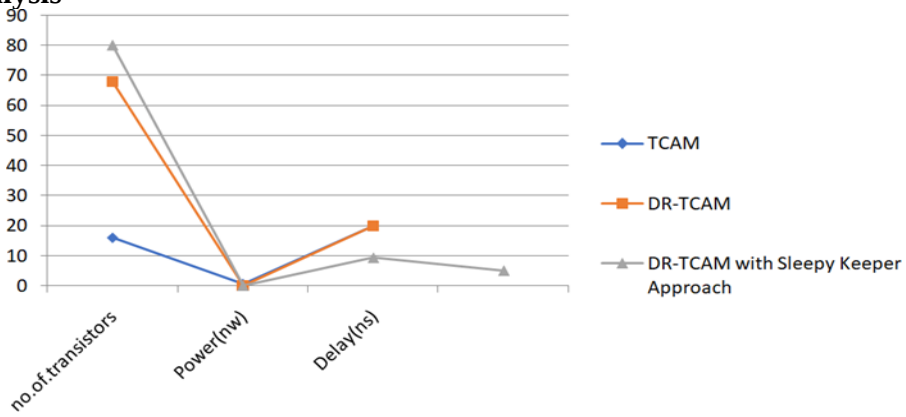
Transient Analysis



Conclusion

This project focuses on the design of a Sleepy Keeper Approach based DATA RETENTION TCAM. The primary purpose of this DR-TCAM is to compare the input search with the data stored in memory and output the matched data. The development of the sleepy keeper Approach as a strategy integrated into the DR-TCAM architecture presents a promising solution to mitigate the significant power consumption associated with traditional TCAM designs. Also we aimed to enhance the power-saving capabilities of DR-TCAM implementations while ensuring the integrity of mask data, a critical aspect in routing table operations. Moreover, by implementing the sleepy keeper Approach, we ensure that our data remains safe and intact, even if the power goes out. This means we won't lose any important information during unexpected shutdowns or outages.

REFERENCES

[1]Yen-Jen Chang , Member, IEEE, Kun-Lin Tsai , Member, IEEE, and Yu-Cheng Cheng " Data retention based low leakage power TCAM for network packet routing " EEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 68, NO. 2, FEBRUARY 2021
[2]N. Mohan and M. Sachdev, “Low-leakage storage cells for ternary con-tent addressable memories,”IEEETrans.VeryLargeScaleInteger.(VLSI)Syst.,vol.17,no.5,pp.604–612,May 2009.
[3]T.-S.Chen,D.-Y.Lee,T.-T.Liu,andA.-Y.Wu,“Filter-baseddual-voltagearchitecturefor lowpowerlong- wordTCAMdesign,”inProc.2ndInt.Conf.Intell. Green Build. Smart Grid (IGBSG), Jun. 2016, pp. 1–5.
[4]Y.-J.Chang,“UsingthedynamicpowersourcetechniquetoreduceTCAMleakagepower,”IEEETrans. CircuitsSyst. II,Exp. Briefs,vol. 57,no. 11, pp. 888–892, Nov. 2010.
[5]Y.-J.Chang, K.-L.Tsai, andH.-J.Tsai, “Low leakage TCAM for IP look up using two-side self-gating,”IEEETrans.CircuitsSyst.I,Reg.Papers,vol.60,no.6,pp.1478–1486,Jun.2013.
[6]Y.-C. Cheng, J.-H. Chen, T.-C. Wu, and Y.-J. Chang, “Low leakage mask vertical control TCAM for network router,” in Proc.IEEE Asia–Pac.Conf.CircuitsSyst. (APCCAS),Oct.2016, pp.469–472.
[7]W.Zhang,L.Li,andJ.Hu, “Design techniques of P-type CMOS circuits for gate-leakage reduction in deep sub-micron ICs,” in Proc. IEEE 52nd Int. Midwest Symp. Circuits Syst. (MWSCAS), Aug. 2009, pp.551–554.