Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 6, June : 2024

PSEUDO PRECHARGE FREE TERNARY CONTENT ADDRESSBLE MEMORY

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ABSTRACT
CAM(Content Addressble Memory) is a hardware search engine in which the access is performed on the basis of contents rather than physical address.In CAM there is no need of address location to be known for writing data into memory and retrieving data from the memory when compared to RAM**.** BICAM (Binary Content Addressable Memory): BICAM is a type of memory that allows for parallel search operations. In BICAM, each memory cell stores a single bit, and the memory is organized such that the content of the memory cells is compared in parallel with a search key. BICAM is commonly used in applications where fast search operations are crucial, such as network routers, database systems, and content-addressable memory (CAM) architectures. TCAM (Ternary Content Addressable Memory): TCAM is a specialized type of memory that allows for searching based on ternary logic, which means each memory cell can store one of three states: 0, 1, or "don't care" (X). This allows TCAM to perform complex matching operations where multiple search conditions need to be checked simultaneously. TCAM is widely used in networking equipment for tasks such as access control lists (ACLs), quality of service (QoS) classification, and routing table lookups.

Key Words:
Match line, Search line, Control unit, Search speed, Precharge free, CAM array, Clock and timing circuit, Energy efficiency

INTRODUCTION

CAM(Content Addressable Memory) is a type of computer memory that enables data retrieval based on its content rather than the memory address, it performs a parallel search across the rows in an array and provides the search results in a single clock cycle. Each memory cell in CAM stores both data and associated address. CAM compares the input data with stored content in all the cells in a parallel way and it gives the result as a match or mismatch condition.
CAM's(Content Addressable Memory**)** are two types. They are:
1.BCAM(Binary Content Addressable Memory)
2.TCAM(Ternary Content Addressable Memory)
Both CAM's are content addressable memories. CAMs are used in various application like routers, image processing and also provides fast efficient data. BCAM stores and retrieves data using binary logic where each memory cell holds only two values either 0 or 1 but in TCAM it operates on ternary logic which includes three states: they are 0,1 and X (don't care) or wild card operation. When BCAM searches the data with stored content it matches exact condition but in TCAM if one bit is not matched it can take either as X (don't care) either 0 or 1.
If the data was matched with stored content it will gives as a match condition(1) otherwise it shows mismatch condition(0) . In TCAM while data was searching with stored content only two bits are matched if third bit was mismatched then we will consider as X (don't care or wild card operation. But in BICAM the operation was performed faster then TCAM because in BCAM only two bits operation was performed. In BICM flexibility was less than TCAM due to its binary nature there is no don't care operation. TCAM was having more flexibility in handling complex search condition.

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LITERATURE SURVEY

[1] A 10T, 0.22fJ/Bit/Search Mixed-VT Pseudo Precharge-Free Content Addressable Memory: Diptesh Datta , Neelam Surana , Anoop Kumar, and Joycee Mekie , Member, IEEE.

This paper initially gives an understanding of CAM, Content Addressable Memories (CAMs) are high speed hardware search engines that simultaneously perform a parallel search across the rows. This high speed comes at the cost of increased power. In CAMs, most of the power is consumed in the matchlines. Although precharge free CAMs eliminate the excessive power consumption due to the matchlines, they are comparatively slower than conventional CAMs. Further, our extensive Monte-Carlo (MC) simulation results show that existing precharge -free CAMs give false search results under process variations. In this brief, we propose a robust and energy-efficient pseudo-precharge free CAM.

[2] T. V. Mahendra, S. W. Hussain, S. Mishra, and A. Dandapat, "Precharge free dynamic content addressable memory," Electron. Lett., vol. 54, no. 9, pp. 556–558, 2018.

In this it focuses on the precharge free operations techniques and advantages, the design details of this circuit includes NAND-type ML, except that the pass transistor is excluded. If the search bit matches the stored bit, then ML will get charge either from D or D; else, ML will be isolated from both D and D. During the search operation, the search data is loaded in 'SL' and 'SLB'. Since the output at node 'S' arrives through 7 the NMOS transistors, so it passes a perfect logic '0' but a degraded logic '1'.Therefore whenever Q matches with SL, the voltage received at the node 'S' is (VDD-|Vtn|), where |Vtn| is the threshold voltage of the NMOS transistor. In the case of a mismatch, node 'S' outputs a perfect logic '0'. The PPFC design has been optimized carefully for performance, and in this section, we highlight each of them. Firstly, we have enhanced the performance of PPFC by carefully selecting the transistors required in PPFC it enhances search operation becomes faster, and leakage is reduced during hold operation. This comes at the cost of increased write delay,but since CAMs are written only once before they are used, this delay can be easily amortized by the gains obtained dueto increased search speed.

[3] M. Zackriya V and H. M. Kittur, "Precharge-free, low-power content addressable memory," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 8, pp. 2614–2621, Aug. 2016.

The Precharge - Free Ternary content addressable memory (TCAM) is introduced for low-power and high-speed search applications. Elimination of precharge prior to search allows hardware engine to perform more number of searches within the stipulated time. The proposed TCAM cell not only removes precharge of matchline (ML) but also utilises decoupling of bitline and searchline so that unwanted capacitive couplings are minimized at charge storage nodes. A 512 bit of the proposed scheme is implemented using 45 nm CMOS technology and its efficacy is verified and proved through rigorous variations with 1000-point Monte-Carlo sampling of ML voltage as well as multi search dissipation analysis.

EXISTING METHOD

In the NOR type CAM cells if searching data was matched with stored data then ML will be high (1) it remains constant at VDD otherwise if ML is mismatched it will be discharges to 0. Since data in exactly one-row matches the searched data, only one ML remains at V*DD* and all other MLs discharge to '0'. So, before the next search operation, all the (n-1) rows need to be precharged again to V*DD*, which accounts for a high activity factor. Also, since ML is a shared signal across the row, it has a large capacitance. Hence, substantial power is dissipated in charging and discharging of matchlines . So it consists more power consumption, due to this Precharge Free CAM was proposed by Zackriya and Kittur . In precharge Free CAM, there is no need for a separate precharge operation before searching the data or a bit. In Precharge free CAM three operations were performed they are read, write, and search operations.

So power was reduced when compared to NOR type CAM cell. If N is large, the voltage received at the end of ML is '0' (N- number of bits in a row) .We contemplate that this issue was probably not

Industrial Engineering Journal
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observed by the authors of as they had implemented a smaller CAM array of size 4 × 2. Due to those limitations Diptesh Datta, Anoop Kumar, Neelam Surana were proposed Pseudo Precharge Free CAM. We exists 4T CAM Cell by using Pseudo Precharge Free BCAM Cell , this cell stores only two bits either 0 or 1. If WL(write logic)=1, BL(Bit Line)=1, BLB=0 then Q=1 and QB=0. There was no writing done during the search operation and no searching during the write operation. In writing operation values are stored in Q and QB in searching operation if SL=1 and SLB=0 then transistor (T2) transistor will be ON and T1 transistor will be OFF then output is S=0 ,ML will be high(1) it was a match condition. If SL = 0, SLB=1 then the transistor(T2) will be OFF condition and transistor (T1) will be ON condition then output of S=1 ,ML will be low(0) it was a mismatch condition.

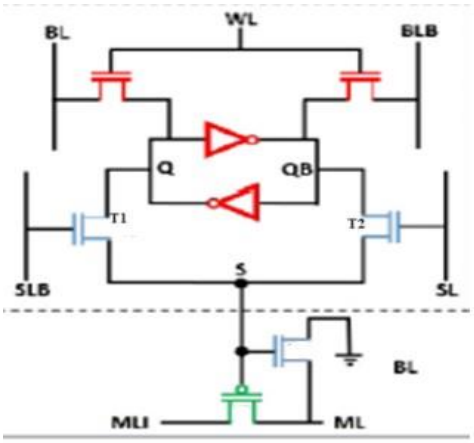

Fig 1 : Schematic of 8T CAM Cell

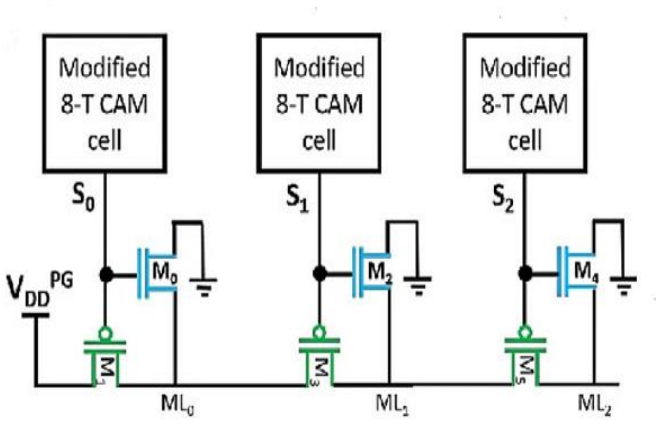

Fig 2 : Array structure of Precharge Free CAM

PROPOSED METHOD

TCAM(Ternary Content Addressa ble Memory) provide additional don't care(X) bit in storage as well as comparison. Search through BCAM matches with an exact data pattern for which many possible combinations with single data entry in not possible with it. With the ternary approach, a CAM can perform association with the range of data words and hence this provides benefit to perform association with more possible data (it is not possible with BCAM designs). We exists 4T CAM Cell by using Pseudo Precharge Free TCAM Cell , this cell stores three bits 0 ,1 and don't care(X) or wild operation. If WL(write logic)=1, BL(Bit Line)=1, BLB=0. In writing operation values are stored in Q and QB in searching operation if SL=1 and SLB=0 then transistor (T2) transistor will be ON and T1 transistor will be OFF then output is S=0 ,ML will be high(1) it was a match condition. If SL = 0, SLB=1 then the transistor(T2) will be OFF condition and transistor (T1) will be ON condition then output of S=1 ,ML will be low(0) it was a mismatch condition SL(Search Line)= 1, SLB=0 ,VDD=1 then ML(Match Line)=1 it was a match condition if ML=0 is was a mismatch condition. There was no writing done during the search operation and no searching during the write operation. If SL =1, SLB=1 then output of S will be taken as X it means (either 0 or 1).

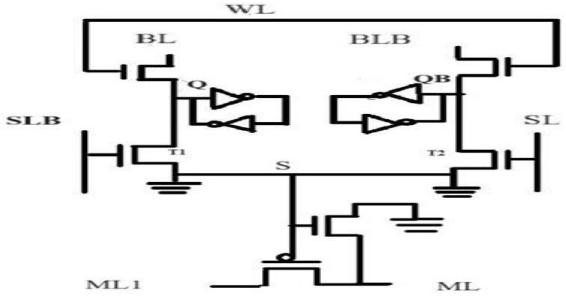

Fig 3 : Schematic of TCAM Cell

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 6, June : 2024

If the output of S is taken as 0 (S=0) then ML will be high(1) it was a match condition or S=1 then ML will be low(0) it was a mismatch condition

There was no writing done during the search operation and no searching during the write operation. If SL =1, SLB=1 then output of S will be taken as X it means (either 0 or 1). If the output of S is taken as 0 (S=0) then ML will be high(1) it was a match condition or S=1 then ML will be low(0) it was a mismatch condition.

SL	SLbar	Q Qbar	ML
0	1	01	Miss match
1	0		Match
0	1	10	Miss match
1	0		Match
0	1	11	Wild match
1	0		

Fig : Truth table of TCAM

DESIGN STRUCTURE OF TCAM

Ternary Content Addressable Memory (TCAM) is a specialized type of memory used in networking devices for high-speed table lookups TCAM is composed of individual cells, each capable of storing a ternary value (0, 1, or don't care 'X'). This ternary nature is what sets TCAM apart from traditional RAM or ROM, where each bit is either 0 or 1.Word Lines and Bit Lines. Like in RAM, TCAM has word lines (rows) and bit lines (columns). Word lines select a row of cells, while bit lines select a column and introduces match lines, which are associated with each word line. When a search is performed, match lines signal whether there's a match between the input and the stored data in that row. The comparison logic allows for searching using ternary masks. For example, in an IPv4 routing table, if the search key is "1001X", the 'X' indicates a don't-care bit. It often includes priority encoding logic. If multiple matches are found, it can prioritize them based on pre-defined rules. This is crucial in networking applications where routing decisions need to be made efficiently. It operates in parallel, allowing for fast searches across a large number of entries simultaneously. TCAM's control logic manages read, write, and search operations efficiently. It coordinates the activation of word lines, bit lines, match lines, and comparison circuits as per the given instructions. Overall, TCAM's design is optimized for high-speed content-based searches, making it suitable for tasks where traditional memory structures would be too slow or inefficient.

RESULT ANALYSIS

The schematic circuit of TCAM was designed in Tanner tools with 45nm technology. TCAM is simulated with the supply voltage of 1V. Although BCAM has less power consumption and delay when compared to TCAM, it was advance technology and very useful for complex searching operations.

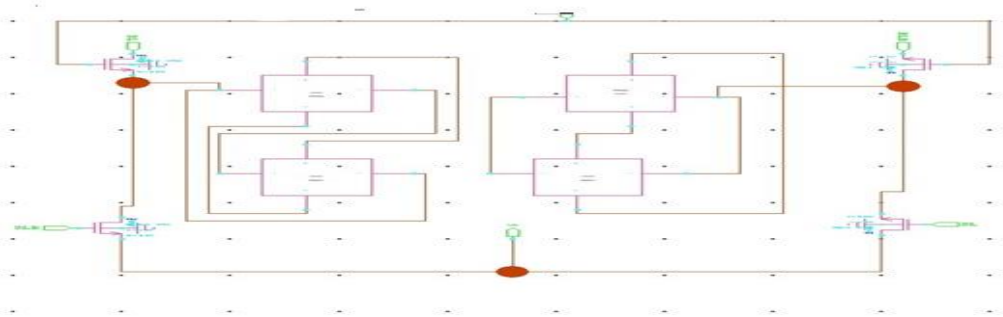

Fig 4: Schematic of NOR TCAM

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 6, June : 2024

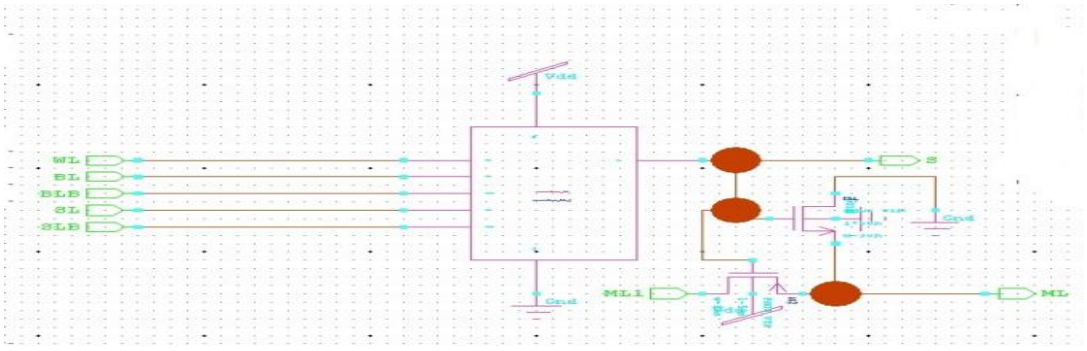

Fig 5: 1bit TCAM Cell

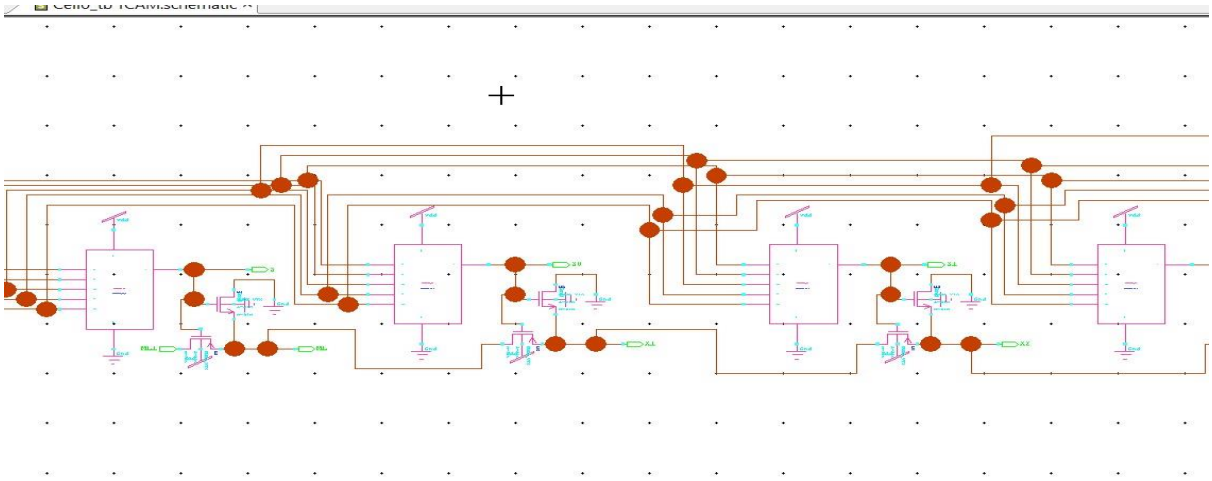

Fig 6: 4bit TCAM Cell

RESULTS OF TCAM

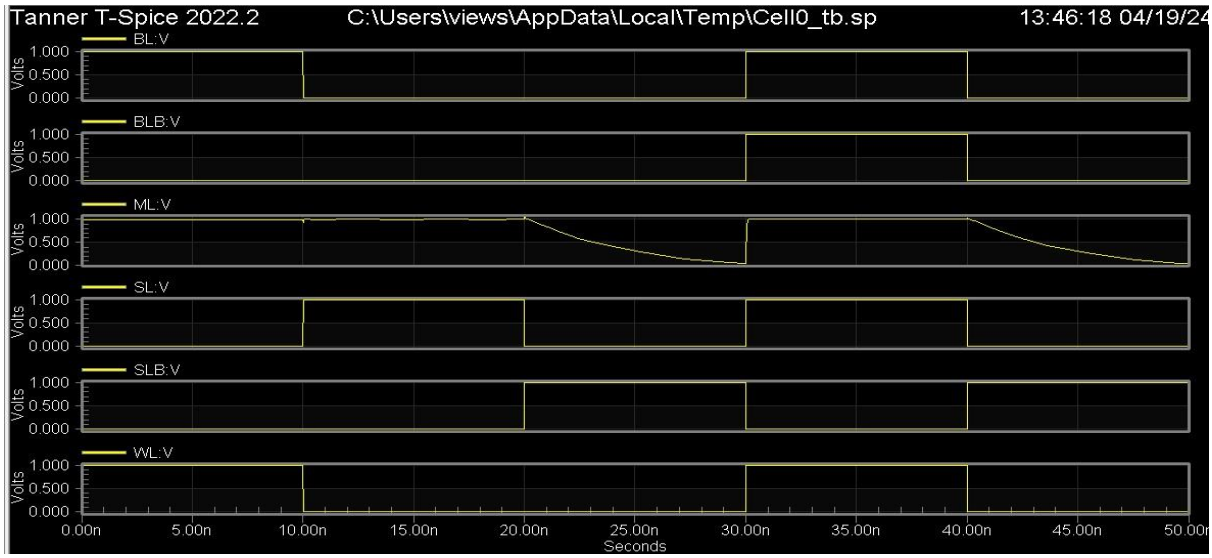

Fig 7: 1 BIT output

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ISSN: 0970-2555
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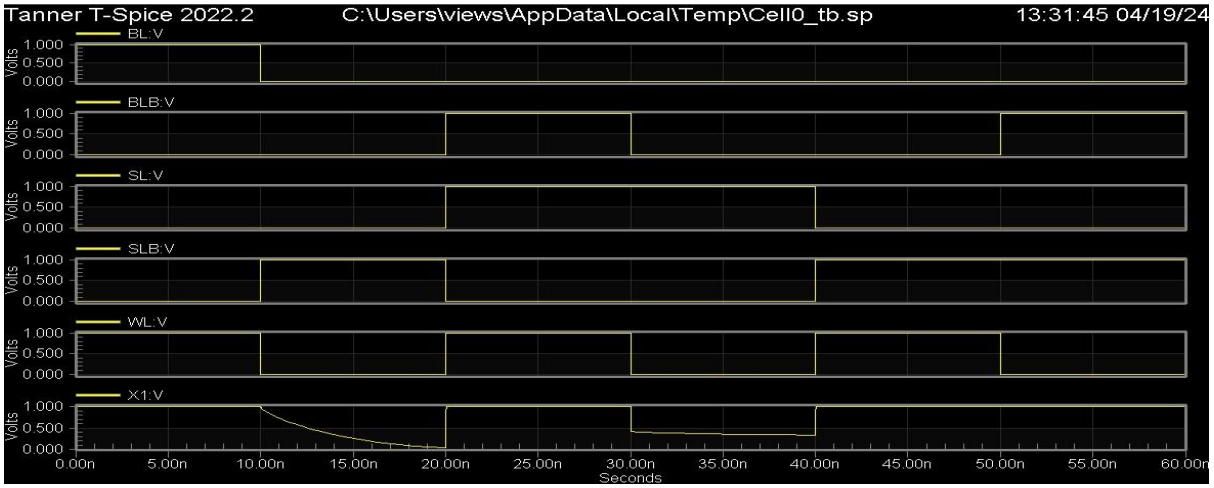

Fig 8: 2 BIT output

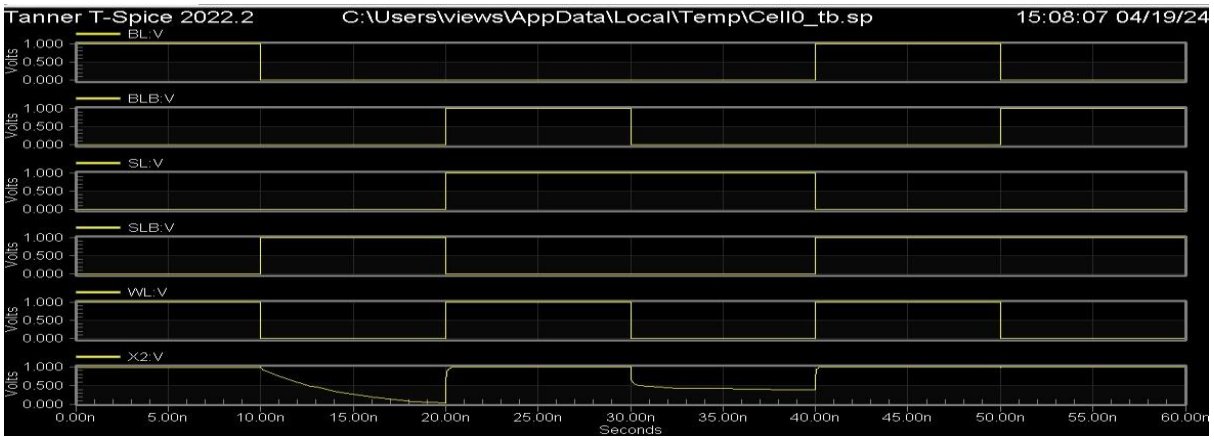

Fig 9: 3 BIT output

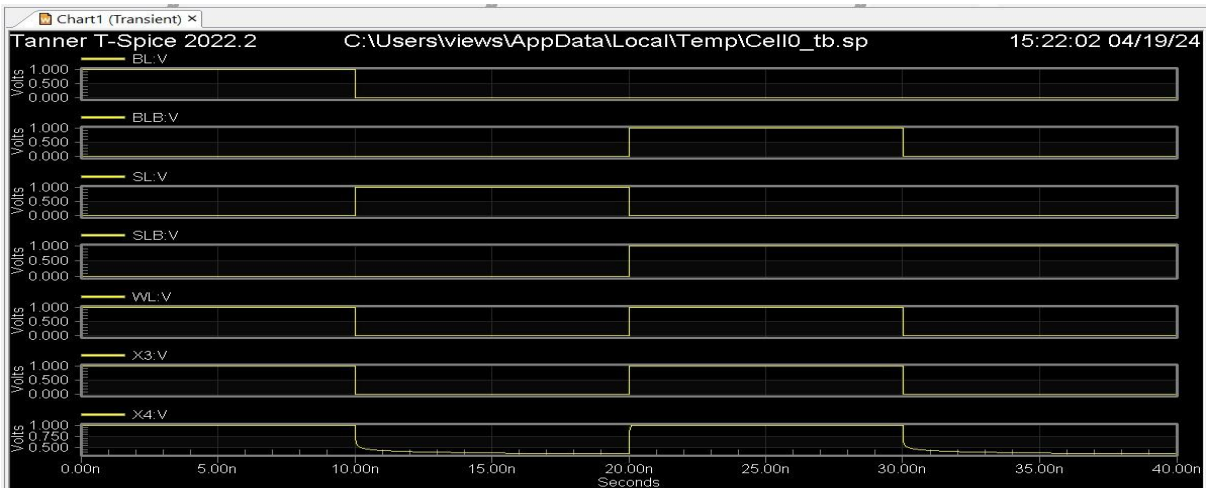

Fig 10: 4 BIT output

S.NO	BICAM	TCAM	BICAM	TCAM
	Power consumption	Power consumption	Delay	Delay
1bit	0.0350µWatts	0.1970µWatts	21.1ns	26.21 ns
2bit	0.1289µWatts	0.2004µWatts	21.98 ns	26.3 ns
3bit	0.135µWatts	0.283µWatts	21.7 ns	25.86 ns

4bit	0.429µWatts	0.5723µWatts	20.2 ns	25.2 ns

CONCLUSION

In conclusion, Pseudo Precharge-Free BiCAM (PPF-BiCAM) and Pseudo Precharge-Free TCAM (PPF-TCAM) represent significant advancements in content addressable memory (CAM) technology, offering a range of benefits over traditional CAM architectures. These innovations have the potential to revolutionize memory design in various computing applications, from networking and telecommunications to high-performance computing and beyond. By eliminating the precharge and restore phases inherent in traditional CAM designs, PPF-BiCAM and PPF-TCAM achieve remarkable reductions in power consumption and access latency. This not only improves energy efficiency but also enhances overall system performance, making them well-suited for demanding real-time applications where speed and responsiveness are critical.

Moreover, the simplified design of PPF-BiCAM and PPF-TCAM contributes to lower complexity, reduced area overhead, and potentially lower manufacturing costs. This scalability and cost-effectiveness make them attractive options for integration into a wide range of systems, from embedded devices to large-scale data centers . Additionally, the improved reliability and robustness of PPF-BICAM and PPF-TCAM offer enhanced system uptime and lower maintenance requirements, further bolstering their appeal in mission-critical environments. In summary, Pseudo Precharge-Free BICAM and Pseudo Precharge-Free TCAM represent cutting-edge solutions that address key challenges in contemporary computing systems. Their combination of reduced power consumption, improved performance, simplified design, scalability, and reliability make them formidable contenders in the ever-evolving landscape of memory technologies, poised to shape the future of computing in diverse applications and industries.

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