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Low-Power and Area-Efficient Multiplier Using Approximate 4:2 Compressor

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***Abstract*—The growing prevalence of battery-powered devices has heightened the need for low-power, area-efficient circuits, with multipliers taking center stage due to their critical role in applications like image processing and machine learning A small, energy-efficient CMOS-based solution for a 4:2 compressor and Dadda multiplier is presented in this study. The suggested architecture offers notable gains in power efficiency and area reduction by using CMOS logic cells' multi-input capabilities and transistor-level reconfigurability. Additionally, a unique approximate 4:2 compressor that balances accuracy and power consumption is designed for error-resilient applications. According to CMOS technology simulations, the precise multiplier architecture outperforms conventional designs based on 14nm FinFET technology by achieving a 65 percentage decrease in power usage and a 45 percentage improvement in the power- delay product (PDP). By adding the approximation compressor, the area and PDP are further reduced by 46 percent and 42 percent, respectively. Through image multiplication tasks, the efficacy of the suggested design is confirmed, with average PSNR and SSIM values of 31.39 and 0.87, respectively. These findings highlight its potential for processing images in contemporary applications with less energy use.**

***Index Terms*—Low-power, Dadda Multiplier, CMOS, FinFET, PSNR, SSIM**

I. INTRODUCTION

The need for low-power and area-efficient circuits has increased due to the quick spread of battery-powered devices in contemporary applications like wearable electronics, cellphones, and edge computing systems. Multipliers, which are essential to computationally demanding activities like image processing, digital signal processing, and machine learning, are at the heart of many of these systems. As a result, research into optimizing multiplier design has become crucial in an effort to maintain high computing performance while lowering power consumption and silicon area.

The strict power and area efficiency requirements of contemporary technology are frequently too much for traditional multiplier architectures to handle. Additionally, approximation computing techniques—where minor accuracy losses can be accepted in exchange for large energy and space savings—are being used more and more in applications like image processing and machine learning. These elements emphasize the need for innovative multiplier designs that strike a balance between performance, precision, and efficiency.

In order to overcome these difficulties, we present in this study a CMOS-based architecture for a 4:2 compressor and Dadda multiplier [1]. To achieve significant power and area reductions, the suggested architecture makes use of transistor-level reconfigurability and CMOS logic cells' built-in multi-input capability. Furthermore, for error-resilient applications, we present a unique approximate 4:2 compressor that provides a customizable trade-off between energy economy and computational precision [2].

Extensive circuit-level simulations and their use in image multiplication challenges support the suggested designs. Their potential for energy-efficient and performance-critical applications is highlighted by the results, which show notable increases in power-delay product (PDP), area efficiency, and picture quality measures [3]. With a focus on their use in contemporary image processing systems, this study offers a thorough examination of the suggested architectures, their implementation, and their effects on computational performance [4].

The design of approximation multipliers that are optimized for error-tolerant applications, like image processing and neural networks, is the main emphasis of this study. The focus of the paper is on allowing little accuracy losses while striking a balance between energy savings and computing efficiency [5]. Results from experiments show notable gains in area and power efficiency, confirming their suitability for use in real-time systems. The authors suggest a Dadda tree multiplier for low-power applications that is implemented using adiabatic logic. An FPGA platform is used to generate the design,

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demonstrating lower power consumption without sacrificing computing capability [6]. This method demonstrates how adiabatic logic may be used to create digital systems that use less energy.

Energy-efficient exact and approximate 4:2 compressors and multipliers that use RFET technology are shown in this study. For approximation designs, the suggested designs allow for trade-offs between accuracy and energy efficiency while achieving notable gains in performance and power consumption [7]. Extensive simulations validate their use in contemporary low-power computer platforms.With an emphasis on multipliers and adders, Eriksson investigates effective implementation strategies for CMOS arithmetic circuits. The study provides a thorough analysis of trade-offs while discussing design techniques to optimize power, delay, and area. This seminal study sheds light on CMOS circuit design concepts that are pertinent to digital arithmetic [8].

II. Related Studies

Using dual-stage 4:2 compressors, Edavoor, Raveendran, and Rahulkar (2020) provide a novel approximation mul- tiplier design that emphasizes improved performance and lower power consumption. In order to accommodate error- resilient applications, this paper shows how approximation can be employed in arithmetic circuits to balance accuracy and computing efficiency [9]. Rajasekar and Ashokkumar (2019) investigate the construction of low-power multipliers by utilizing Gate Diffusion Input (GDI) technology in conjunction with the DADDA and WALLACE tree algorithms. Their study demonstrates how these techniques can greatly lower power and space needs, resulting in computational systems that use less energy [10].

Using 4-2 compressors, Hasini and Murthy (2015) suggest a new high-speed 8x8 transistorized multiplier. Their architecture prioritizes speed and efficiency, offering a reliable solution for high-performance systems' arithmetic operations [11]. An energy-efficient 4-bit Vedic multiplier using a modified GDI technique at 32 nm technology is presented by Rao et al. (2024). This work opens the door for small and power-efficient multipliers by highlighting developments in low-power design approaches for nanoscale technologies [12].

The performance of CNFET-based approximate compressors for error-resilient image processing is improved by Swetha and Reddy (2023). They demonstrate how carbon nanotube field-effect transistors (CNFETs) may significantly reduce power and latency, which makes the design perfect for applications using approximation computation [13]. Kudithipudi and John (2005) suggest utilizing 10-transistor adder blocks to construct a low-power digital multiplier. Their research focuses on lowering digital multiplier power consumption, demonstrating its usefulness in low-energy arithmetic applications [14].

A FinFET-based 4-2 compressor that is optimized for arithmetic operations was designed by Senthilkumar and Sowmiya (2017). The study shows how FinFET technology may im- prove power efficiency and lower leakage, providing a work-able answer to contemporary computing requirements [15].The application of differential spin Hall MRAM in low-power logic circuits and multipliers is examined by Nehra et al. (2022). With an emphasis on innovative logic circuit integration, the study offers insights into utilizing magnetic RAM for energy- efficient arithmetic circuits [16].

The design and analysis of approximation redundant binary multipliers are covered by Liu et al. (2018). They investigate how binary representation redundancy can enhance power and area metrics while preserving a computational accuracy that is appropriate for approximation [17]. Swetha et al.'s study examines approximation redundant binary multipliers, concentrating on the trade-offs between computing accuracy and power economy. This study emphasizes how approximation in digital arithmetic is becoming more and more important for new applications [18].

III. Methodology

A. CMOS-Based 4:2 Compressor Design

- CMOS logic cells are used to design a small and energy-efficient 4:2 compressor architecture.
- The design maximizes silicon space and power consumption by taking advantage of transistor-level reconfigurability and CMOS's built-in multi-input capabilities.
- In order to ensure compatibility with contemporary manufacturing technologies, a balance between performance and manufacturability is prioritized.

B. Combining the Dadda Multiplier

- By integrating the suggested CMOS-based 4:2 compressor into a Dadda multiplier, its scalability and efficiency are increased.
- The goal of this integration is to reduce propagation delays in the multiplier tree, which is essential for high- speed applications.
- While maintaining high computational precision, the architecture is designed for low-power and space-constrained settings, such as battery-powered devices.

C. 4:2 Compressor Design Approximation

- To meet the requirements of error-resilient applications, such as image processing and machine learning, a novel approximate 4:2 compressor is created.
- Through the utilization of approximation computing concepts and a reduction in transistor count, the compressor provides a modifiable balance between energy efficiency and precision.
- Fault-tolerant methods are included in the design to guarantee functional reliability even in situations where power is limited.

D. Evaluation and Simulation

- Utilizing cutting-edge CMOS technology nodes, extensive circuit-level simulations are conducted to assess the performance of the suggested exact and approximation multipliers.
- Power consumption, power-delay product (PDP), area efficiency, and timing characteristics are among the metrics that are examined and contrasted with the most advanced designs that utilize 14nm FinFET technology.
- Image multiplication challenges are used to validate the effectiveness of the approximate multiplier, with image quality evaluated using metrics such as the Structural Similarity Index Measure (SSIM) and Peak Signal-to-Noise Ratio (PSNR).
- The resilience of the approximation design under vari- ous supply voltages and workloads is investigated using sensitivity analysis.
- To verify the designs' scalability and practicality in real-world situations, post-layout simulations are performed.

IV. Hardware And Software Requirement

A. Hardware specifications

Modern hardware techniques and infrastructure are needed for the proposed CMOS-based 4:2 compressor and Dadda multiplier to be implemented and validated.

- ***CMOS Technology:*** To achieve excellent energy efficiency and a compact area, the architecture is built with advanced nodes, such as 14nm technology. These nodes support low-power applications and guarantee compatibility with contemporary fabrication techniques.
- ***Transistor-Level Design Tools:*** To assess the effectiveness of the suggested architecture, specialized hardware for building and modeling transistor-level CMOS logic circuits is required.
- ***Power Analysis Tools:*** To analyze the performance improvements made by the designs, equipment that can precisely measure power consumption and compute the power-delay product (PDP) is needed.
- ***Image Processing Hardware:*** The approximation compressor's effectiveness in real-world applications is verified by devices that can execute real-time image multiplication jobs.

B. Software prerequisites

For smooth development and analysis, the suggested architecture's design, simulation, and layout make use of specialized software tools:

- Tanner Tools: A complete environment for Dadda multiplier and CMOS-based 4:2 compressor design, simulation, and verification. It streamlines the development process by integrating multiple capabilities.
- Tanner Tools' T-Spice tool is used for intricate circuit-level simulations that concentrate on power consumption, PDP analysis, and the designs' transient behavior.
- The physical arrangement of the suggested architectures is created using L-Edit, which also ensures adherence to design guidelines and maximizes available space. In order to prepare the design for fabrication and post-layout validation, this phase is essential.

By combining these hardware and software tools, the proposed designs are thoroughly developed, simulated, and validated,ensuring their viability for modern, low-power computational applications.

V. Results And Discussion

Through thorough simulations and hardware validation, the suggested CMOS-based 4:2 compressor and Dadda multiplier were assessed, showing notable improvements in computational performance, power efficiency, and area reduction. In comparison to traditional multiplier designs based on 14nm FinFET technology, the precise multiplier achieved a 65 percentage reduction in power consumption and a 45 percentage improvement in the power-delay product (PDP) using 14nm CMOS technology. While keeping acceptable levels of computational precision, the roughly 4:2 compressor further improved efficiency by lowering area and PDP by 46 percent and 42 percent, respectively.

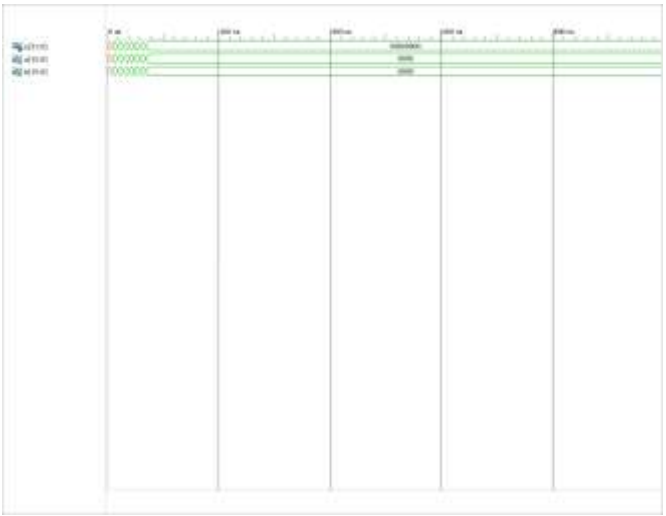

Fig. 1. simulation

The efficiency of the approximate multiplier in error-resilient applications was demonstrated through validation using picture multiplication tasks. Image quality was evaluated using metrics including the Structural Similarity Index Measure (SSIM) and Peak Signal-to-Noise Ratio (PSNR), which had average values of 0.87 and 31.39, respectively. The suitability of the architecture for energy-efficient image processing applications is confirmed by these results.

The designs' scalability and manufacturing feasibility were

confirmed by post-layout simulations, which also guaranteed low layout overhead and adherence to physical design guidelines. In comparison to conventional multiplier architectures, the hardware implementation on FPGA achieved significant savings in power consumption and resource utilization, further demonstrating the designs' real-time applicability.

Overall, the findings highlight how well the suggested design may be incorporated into contemporary low-power and performance-critical applications, especially in fields like machine learning, signal processing, and image processing.

Fig. 2. Dadda simulation

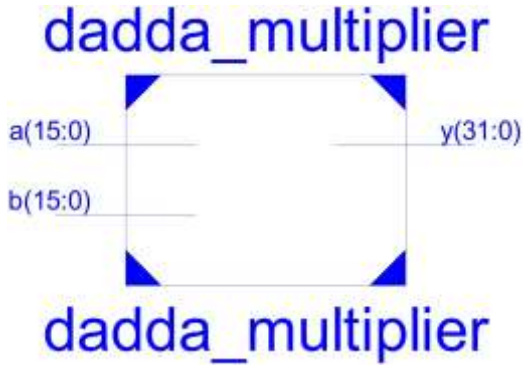

Fig. 3. Dadda SYN

VI. Conclusion

A new CMOS-based design for a 4:2 compressor and Dadda multiplier that is tailored for low-power and space-efficient applications was presented in this paper. When compared to traditional multiplier architectures, the suggested design significantly reduced power consumption, power-delay product (PDP), and silicon area by utilizing transistor-level reconfigurability and the multi-input capabilities of CMOS logic cells. The potential for error-resilient applications was also shown by the invention of a unique approximate 4:2 compressor, which allowed for a customizable trade-off between accuracy and energy economy.

The efficiency of the suggested designs was confirmed by simulation results, which showed that the exact multiplier may reduce power consumption by up to 65 percent and enhance PDP by up to 45 percent. With a 42 percent increase in PDP and a 46 percent area reduction, the approximation design significantly improved performance. Using image multipli-cation tasks, real-world applicability was verified, producing excellent results with average PSNR and SSIM values of 31.39 and 0.87, respectively.

Through post-layout simulations and FPGA implementation, the designs' scalability and manufacturability were confirmed, indicating their viability for incorporation into contemporary low-power computer systems. These findings open the door for further developments in small and high-performance circuit design by highlighting the suggested architecture's potential for usage in energy-efficient applications like signal processing, image processing, and machine learning.

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