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INNOVATIVE DESIGN OF VERY LARGE SCALE INTEGRATION (VLSI) FOR APPLICATIONS REQUIRING HIGH PERFORMANCE MULTIPLIERS

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Abstract: Multipliers play a crucial role in many applications of digital signal processing. Researchers have been working hard to develop a multiplier that satisfies the four requirements of modern technology: low power consumption, homogeneous architecture, compact size, and light weight. The research suggests that there are several potential applications for a tiny very large scale integration (VLSI) architecture for a four-bit multiplier optimized for speed and low power consumption. When Dadda mathematical logic is combined with a mixed single-bit full adder, a highly reliable multiplier factor is produced. The method used to determine this multiplier appears to be correct. Route latency is reduced by 65.9 percent when using the proposed multiplier factor, and energy usage is cut by 24.5 percent when compared to the current multipliers. Find the optimal multiplier with the help of the specter virtuosity app. The real multiplier factor should be calculated using the EDA program CADENCE 5.1.0.

Keywords: Multiplier; Dadda Algorithm; Gate diffusion Input (GDI);Pass transistor logic (PTL);CMOS process technology; Cadecne(tool)

1. INTRODUCTION

When processing data in real time, digital systems rely heavily on a component called a multiplier. Efforts are currently being made to reduce the size, power consumption, and processing time of multiplication and division operations. The multiplier reduces all numbers by 25%–35% when used in conjunction with a half adder and a full adder. Digital signal processing (DSP) operations on small sequences are sped up by 40-60% when high-speed Vedic multipliers are used instead of standard multipliers. Since fixed and floating point multipliers were developed using a Vedic technique [3], digital signal processors have improved precision and performance. There have been many different designs and algorithms used to increase efficiency and power. Dadda, Wallace Tree, Vedic, and Booth all provide several examples.

In the following section, the Dadda algorithm will be discussed in detail. The proposed system's design is elaborated upon in Section III.

Section IV of the paper analyzes the data, taking into account both the suggested and actual multipliers. In the concluding fifth chapter, everything is resolved.

2. DADDA ALGORITHM

The suggested research use the Dadda technique to shorten the critical path, hence increasing the multiplier's throughput. The proposed multiplier uses a four-bit representation to perform sixteen independent partial multiplications. Figure 1 depicts an example of grid multiplication using a 4x4 grid and a 4 leaf tree. Get the tree down to just two nodes using the dada approach.

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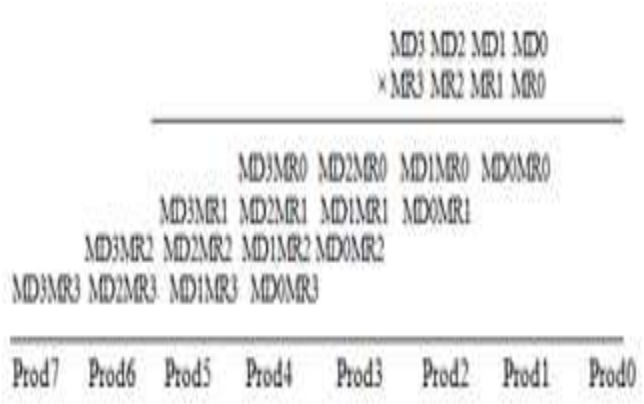

Fig.1. Sample 4×4 Multiplication

The Dadda approach shortens the time it takes for information to spread by minimizing the importance of using previous level outputs when calculating future level outputs. Before the dada approach was employed, the initial level of the tree only had four nodes. Only three remain at this time. The multiplication tree has three levels until the second level, when there are only two levels. As soon as you reach the last stage, the game is compressed from two stages down to one. Figures 2–4 depict the process for decreasing amounts.

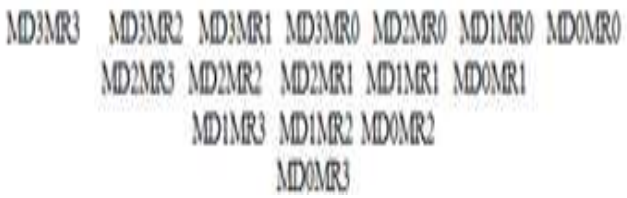

Fig.2. Level -1

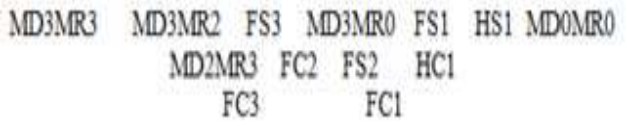

Fig.3. Level -2

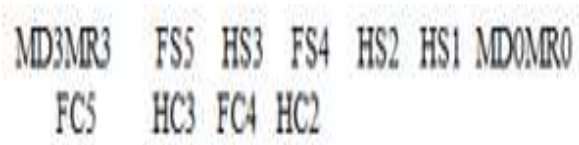

Fig.4. final Level

3. PROPOSED 4×4 MULTIPLIER

The blocks for the 4-by-4 repeater are shown together in Figure 5. The multiplier is made out of a composite pass transistor logic circuit. These circuits are compatible with adders that take in two or three binary digits. The multiplier consists of these circuits. This circuit uses just ten transistors.

The multiplier's first stage consists of sixteen AND logic circuits, which collectively generate and employ sixteen intermediate products.

The second level of the tree can be split in half using either a single binary digit adder circuit with two inputs or three binary digit adder circuits with three inputs. Combining two two-input binary-digit adder circuits and two three-input adder circuits will result in a reduction to the third level. Figure 5 illustrates the use of buffers in the signal path from the amplifier to the load in order to increase the output voltage. The photo clearly demonstrates this.

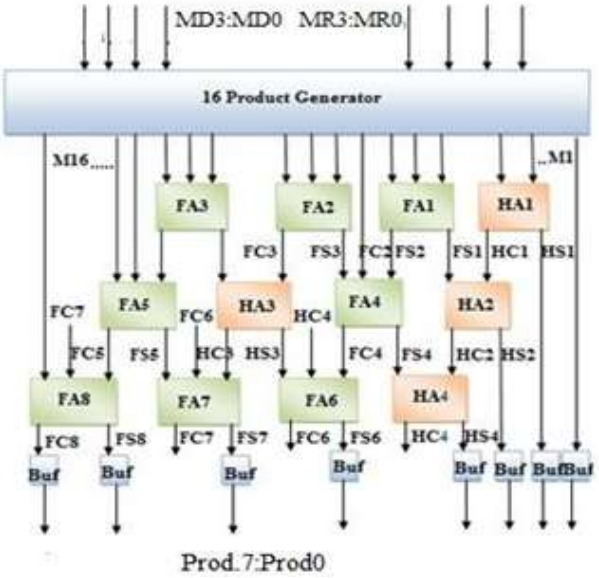

Fig.5. The item under consideration at the moment is a multiplier of 4 times 4.

The proposed architecture consists of eight buffers, eight adder circuits for three-input binary numbers, four adder circuits for two-input binary numbers, and eight adder circuits in total. The AND gate's core component is depicted in Figure

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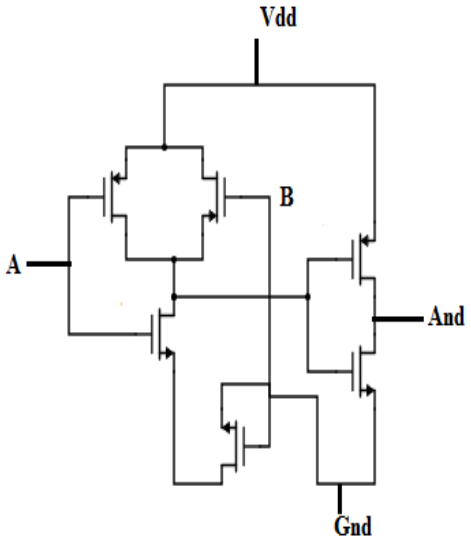

Fig.6. AND Gate

Figure 7 depicts the recommended multiplier for the single adder user's circuit design. T1, T2, and T3 denote the individual pieces. The XOR gate in Module T1 has been modified so that it may be used with Gate Diffusion Logic (commonly known as GDI). Module T2 demonstrates the XOR operation of the PTL, while Module T3 describes the operation of the MUX. The T1 and T2 units each produce a set of results, which are then added together to form the total adder. The T3 module generates a carry output when it is activated.

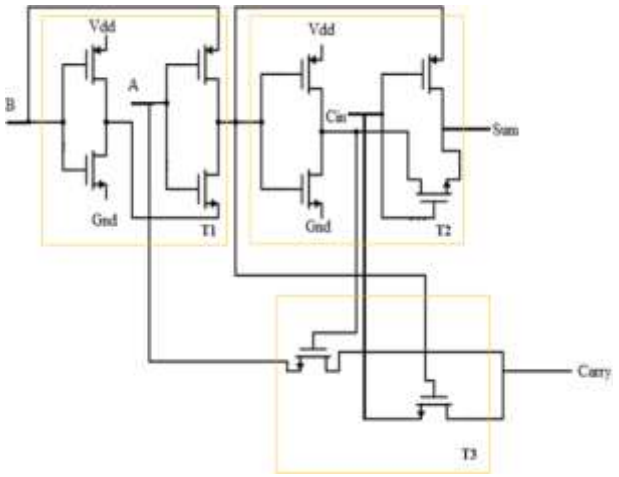

Fig.7. This query depicts a potential architecture for a single-bit full adder.

The addition of binary numbers requires a circuit with two input lines, which is what you'll need to build a multiplier. This component is essential for the instrument to function. For a 4x4 multiplier, you'll need four 2-input binary adder circuits. Figure 8 is a CMOS representation of a binary adder circuit, which accepts two binary values as inputs. This circuit operates on the basis of binary numbers.

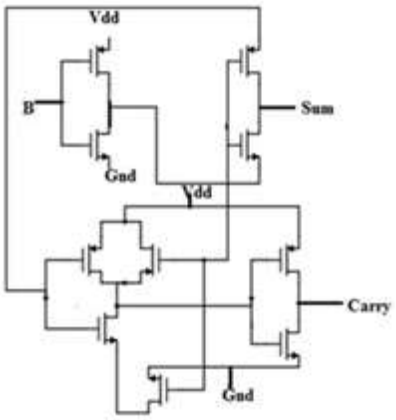

Fig.8. Two input binary digits adder circuit

A multiplier is used to maintain a constant voltage and expedite data transfer between the first and last stages. Figure 9 depicts the data provided.

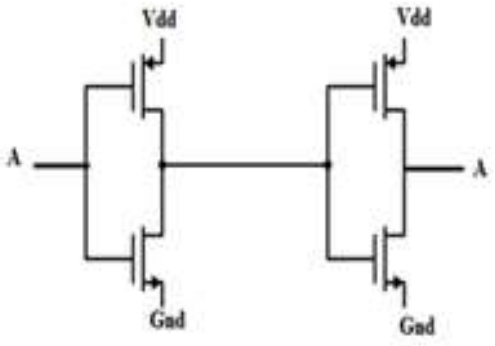

Fig.9.Buffer

4. SIMULATION RESULTS

Programming tool for electrical design CADENCE 5.1.0 is used to create multipliers. On the other hand, Specter Solo can be used to simulate different conditions. As can be seen in Figure 10, the RTL schematic design of the proposed multiplier was created utilizing Cadence software.

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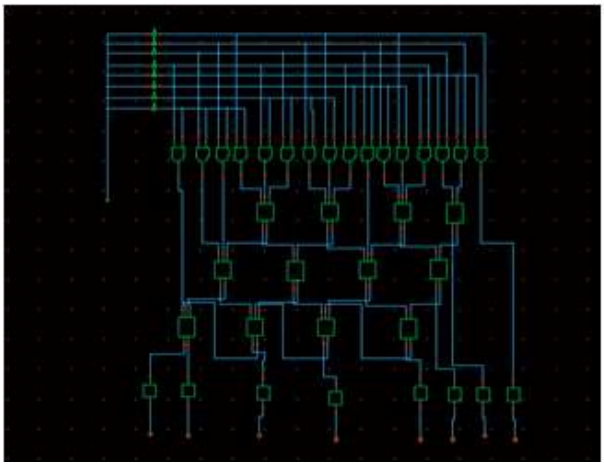

Fig.10. A diagram displaying the technology that was to be employed in the development of the system.

The above graph displays the suggested 4-bit multiplier's sensitivity to changes in the input data. This word "denotes" the multiplier's displayed output, which consists of Prod0, Prod1, Prod2, Prod3, Prod5, Prod6, and Prod7.

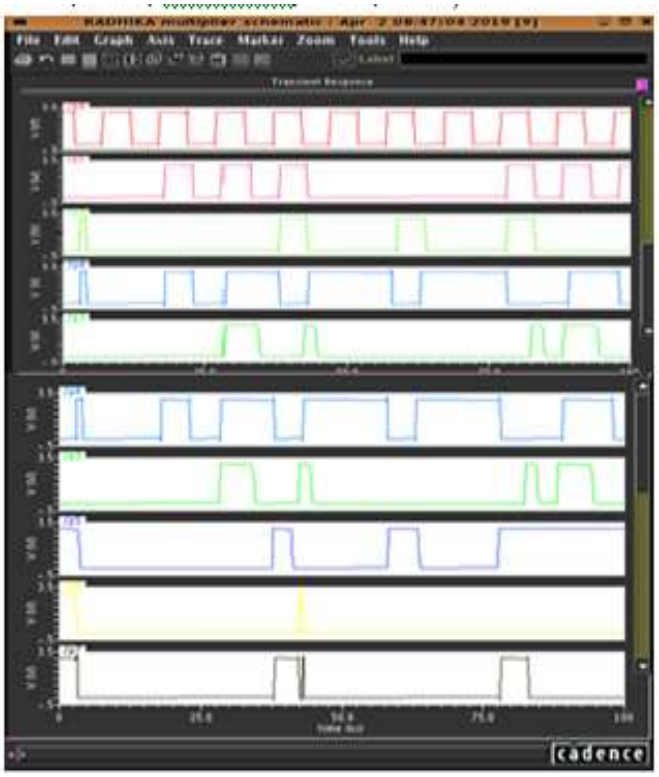

Fig.11.Tranisent response of the multiplier

Below figures shows the power and delay calculation in cadence.

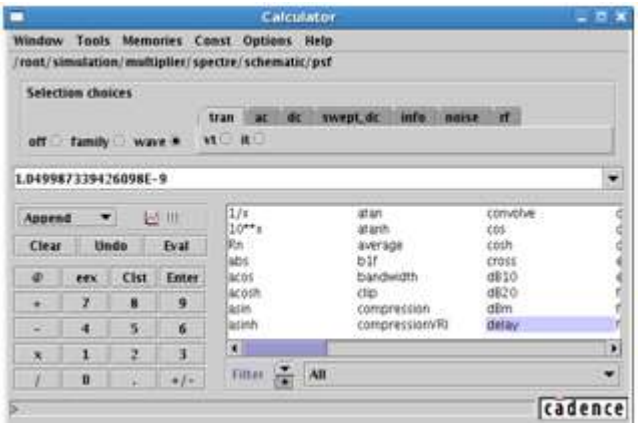

Fig.12.Power calculation in cadence

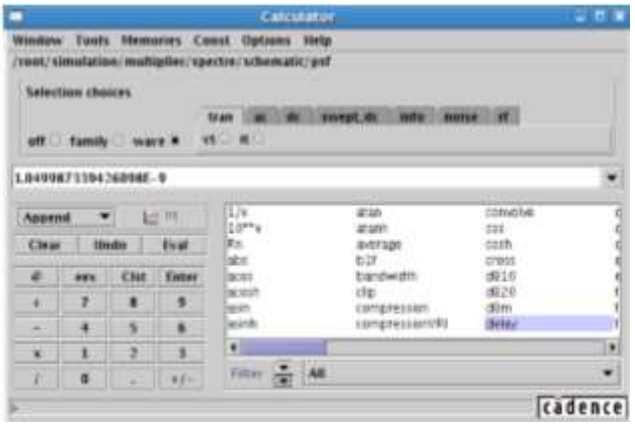

Fig.13.Delay calculation in cadence

Table I. Comparison Of Different Multipliers

No	Multiplier	No of transistors	Power in mW	Delay in ns
1	Using Conventional CMOS Full Adder	392	0.0058	3.834
2	Using Hybrid Full Adder (Existing)	264	0.00224	3.0603
3	4-bit Dadda Multiplier using Compressor	376	1.172	0.353
4	DADDA Tree Multiplier Using Adiabatic Logic	-	77	-
5	4-bit Static CMOS based DADDA Multiplier	316	-	-
6	**Proposed Multiplier**	**248**	**0.00169**	**1.0409**

The efficiency ratios of full adder-based multipliers are tabulated in Table I. This comprises the number of transistors, power consumption, and duration of the critical route. The table displays how the proposed multiplier

simplifies the circuit, reduces power consumption (1.69W), and shortens the critical path.

In the table below, we can see the cadence delay and computational power. The latency of the suggested multiplier, 1.04 ns, is considerably less than the latency of the other multipliers.

Fig.14 and Fig.15 shows the graphical representation of power and delay.

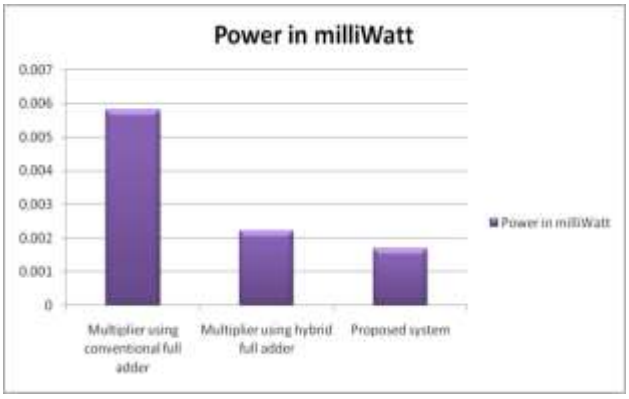

Fig.14. Comparison of power in mW

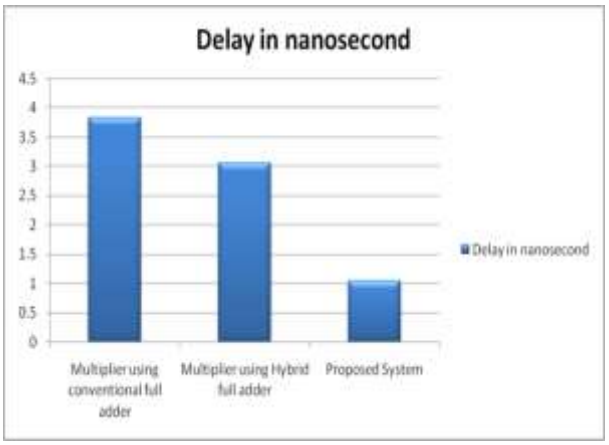

Fig.15.Comparison of delay in nano second

Table II shows the logic utilization of various modules in 4 bit multiplier.

Table II. Logic Utilization Of Various Modules

Module	No of transistors	Technique used
Full adder(area and power efficient single bit full adder)	80	Sum: GDI XOR. Carry: PTL XOR
Half adder	40	CMOS Processtechnology
Buffer	32	CMOS Processtechnology
AND gate	96	CMOS Processtechnology

5. CONCLUSION

The 4-bit multiplier was built using a hybrid device. It can add binary numbers together with its three inputs and one-bit adder. The circuit is functioning perfectly. The objectives of this design are to create the most complex circuit possible while using the least amount of power and experiencing the least amount of delay. PTL and GDI adder circuits are low-power and fast-propagation, making them ideal for operations involving three binary digits. These two additions improve the overall performance of the circuit. A hybrid three-input binary-digit adder circuit is employed to provide the best response time and data transfer speed. Dada is utilized to minimize communication lag. A multiplier with a latency of only 1.04 ns and a factor of 44 was demonstrated. Its average power consumption is estimated to be 1.69 watts. The size is predicted to be less than the size of the conventional repeater.

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