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DESIGN AND PERFORMANCE ANALYSIS OF POWER GATING BASED 6T AND 8T SRAM CELL

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ABSTRACT
Static Random Access Memory (SRAM) is an important element in today's digital systems, but its high power consumption is a challenge to low-power designs with energy efficiency in low-power applications. This work centers on the analysis of 6T and 8T SRAM cell structures with power gating, designed using 90nm CMOS technology, to realize lower power consumption with comparable performance. Power gating works by efficiently reducing leakage by isolating idle circuit blocks, sharply curtailing static power in both 6T and 8T SRAM configurations. Through a comprehensive study of power-gated and non-power-gated 6T and 8T SRAM cells, the effectiveness of power gating is seen to influence power saving, read delay, and stability across different supply voltages. Simulation outcomes prove that power gating significantly reduces power dissipation, with the 8T SRAM enjoying improved read stability because of its independent read and write paths, thus being more dependable for low-voltage applications. Such improved stability makes the power-gated 8T SRAM a better choice for energy-constrained applications, like IoT and mobile devices, where both power efficiency and reliability are essential.The research concludes that power gating provides a strong method for designing energy-efficient SRAM in VLSI systems, and the 8T SRAM offers the best trade-off of power reduction, stability, and performance.
Keywords: SRAM Cell, Power Gating, Energy Efficiency, Delay, Microwind, Dsch3.9

INTRODUCTION
Semiconductor memories have emerged as crucial in VLSI systems during the past decade, being a central component of today's electronic devices. As memory takes up a large proportion of the chip space, its design needs to be optimized to enhance overall efficiency. Scaling the CMOS technology has led to continuous reduction in transistor size, which has increased area density and minimized power consumption, but at the same time has put pressure on developing low-power, high-speed, and stable memory designs [1]. With the increasing demand for energy-efficient equipment, power consumption in SRAM cells has become an acute challenge. Scaling SRAM cells, however, brings in the challenges of decreased stability, increased power consumption, and susceptibility to process variations.
The paper gives a comparison of 6T and 8T SRAM cells, both power-gated and non-power-gated, under the consideration of how much they can save power without compromising stability. Power gating is used to shut off leakage paths during standby, realizing huge saving in static power dissipation. The 8T SRAM

structure improves read stability by isolating read and write operations, and power gating also improves power savings without any impact on functionality [2]. The study investigates how power gating affects read/write margins, power efficiency, and delay performance with respect to conventional non-power-gated SRAM architectures [11]. With 90nm CMOS technology, the new 6T and 8T SRAM cells were simulated, which showed significant power savings and efficiency compared to non-power-gated designs [12]. Power-gated SRAM cells also show higher stability and lower leakage, which makes them suitable for low-power, high-density memory applications [4]. The rest of this paper discusses the history of power gating in SRAM, 6T and 8T SRAM cell design, simulation results, and conclusions of the study.

6T SRAM CELL:

The traditional 6T SRAM is the basic architecture of most SRAM designs. It is composed of six MOSFETs and has three modes: read, write, and hold [4]. The cell contains two cross-coupled inverters, each consisting of four transistors, to hold a single bit, and two access transistors for read and write operations [1]. Data is written via the Bit Line (BL) and its complementary Bit Line Bar (BLB), with storage nodes Q and Q', and M5 and M6 as access transistors [5]. The M1 and M2 are NMOS transistors that function as pull-down devices, and the M3 and M4 are PMOS transistors as pull-up devices. As shown in Fig 1, M1, M3 and M2, M4 make the cross-coupled inverters [13]. The term line (WL) controls the operation of access transistors.

During read mode, information is read out from complementary bit lines. At hold mode, the word line is turned off, leaving the cell in an idle state [2]. In a read operation, turning on the word line activates the access transistors [6]. When the cell contains a '1', a high signal travels on the bit line while a low signal travels on the complementary bit line; the opposite happens for a '0' [7]. The bit line and its complement therefore have opposite signals. A sense/write circuit at the bit line ends senses their states and generates the output. When in hold mode, the access transistors are deactivated and the SRAM stores its data due to a latching effect. Static RAM is widely applied in cache memory applications [8]. Nevertheless, its complicated design renders it more expensive and restricts its capacity for huge volumes of data storage on one chip [9].

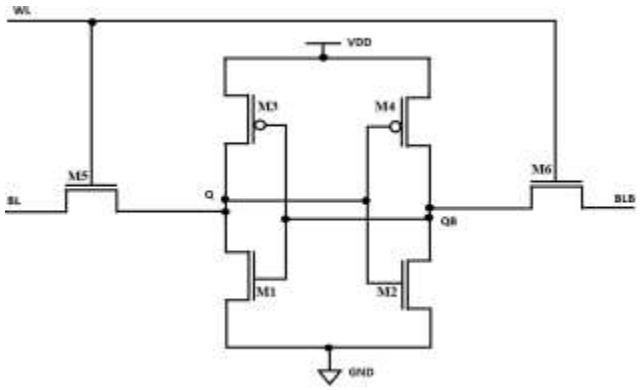

Fig 1: 6T SRAM CELL

A. Power consumption

The energy consumption of an SRAM cell consists of dynamic, static, and leakage power, all of which are essential to ensure energy efficiency. Dynamic power is utilized during read and write operations as a result of switching activities, whereas static power results from leakage currents when the cell is not in operation. As CMOS technology advances, leakage power has emerged as a major contributor in total

power consumption, which has led to the use of strategies such as power gating to make SRAM more efficient [14].

The total power dissipation in an SRAM cell is given by

$$P_{\text{total}} = P_{dy+} P_{st} \text{ ----------(1)}$$

Static and dynamic power dissipation expressions are shown

$$P_{dy} = C \times V^2 \times f \times \alpha \text{----------(2)}$$

$$P_{st} = I_{leak} \times V \text{ ---------- (3)}$$

Where α is the switching activity; f is the operating frequency; C is the load capacitance.

B. delay

SRAM cell delay is a significant parameter in influencing the write and read speed as well as memory performance. Increased bit-line capacitance causes longer charging and discharging times, hence longer read and write delays [5]. The word line activation time dictates the speed of access transistor turning on data transfer, thereby influencing the overall access time [6]. The operation of access transistors, based on their threshold voltage and drive strength, largely influences the speed of operation [8]. Variation of supply voltage and process parameters may also change delay [12]. Delay reduction is necessary for increasing SRAM performance, providing quick and secure memory access for high-speed applications [13].

6T SRAM CELL WITH POWER GATING

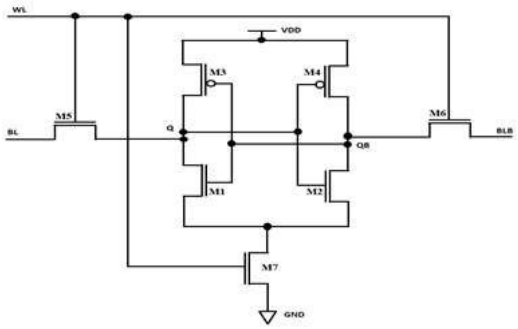

Fig 2: 6T SRAM CELL WITH POWER GATING

In a bid to reduce the depletion width of an SRAM cell, substrate doping concentration has to be increased proportionally [15]. Scaling and junction and gate oxide thickness control is a very powerful means of short-channel effect management, having a direct influence on device dimensions as well as on voltages [4]. Control of doping profile variation in the channel region enables electric field distribution and potential contours to be optimized. The key objective is to improve channel behavior, minimize off-state leakage, and optimize linear and saturation drive currents [5]. All of these techniques serve to minimize leakage at the process level.

At the circuit level, there are various techniques that are used to minimize leakage power, such as self-reverse biasing, multi-threshold voltage designs, multi-channel doping, multi-supply voltage schemes, and dual-supply SRAMs [6]. SRAM cell works in read, write, and hold modes, and leakage power depends on supply voltage, leakage current, and threshold voltage, which are different according to the operating mode [10]. During hold mode, the 6T SRAM cell holds the digital logic values at nodes Q and QB by a cross-coupled inverter pair with positive feedback. During this mode, however, the lower NMOS transistor is in the subthreshold region, establishing a leakage path from the storage node (Q or QB) to ground [16]. This leakage can cause data flipping or loss. As depicted in Fig 2, an extra NMOS transistor is placed between the pull-down NMOS transistors of the inverter pair and ground. This transistor blocks the leakage path, minimizing static power loss during hold mode. In the power-gated 6T SRAM cell, this

extra NMOS transistor is driven by the word line signal [7].

8T SRAM CELL:

The 8T SRAM cell is used to enhance memory stability and reliability over the conventional 6T SRAM. Among the major drawbacks of the 6T SRAM is that it has a common path for read and write, resulting in read disturbance and even data corruption. The 8T SRAM prevents this by using two more transistors to form a dedicated read path, thus promoting read stability and energy efficiency [7]. Separating read and write operations, the 8T SRAM reduces voltage fluctuations at the storage nodes and thus is more efficient and reliable for low-power applications [6].

The 8T SRAM cell has three basic modes of operation: write, read, and hold. In write mode, it is akin to the 6T SRAM, where two cross-coupled inverters hold complementary data at nodes Q and QB. When the word line (WL) is enabled, the write access transistors (N3 and N4) short the storage nodes to the bit lines (BL and BLB), and the data on BL and BLB overwrites the stored data at Q and QB. When WL is disabled, the inverters hold the data through positive feedback [2].

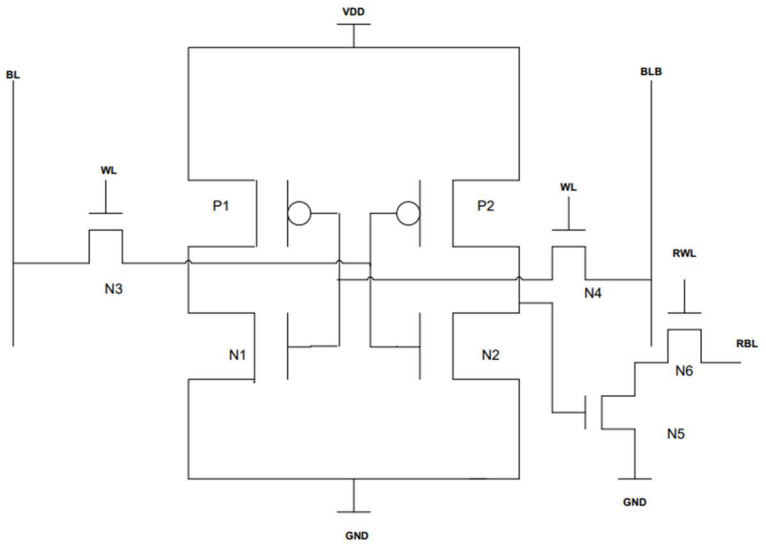

Fig 3: 8T SRAM CELL

A major advantage of the 8T SRAM is its independent read mechanism, which improves stability by separating the read and write paths. In the 6T SRAM, read operations can disturb the storage node voltage, potentially causing read failures. In contrast, the 8T SRAM uses a read word line (RWL) and read bit line (RBL) that are isolated from the write cycle. Before a read operation, RBL is precharged to VDD. When RWL is asserted, the read access transistor (N5) is activated, and the stored value at Q drives the read buffer transistor (N6). If Q is high, N6 turns on, discharging RBL to ground; if Q is low, N6 remains off, and RBL stays at VDD. This ensures that the stored data remains undisturbed during read operations, significantly improving read stability compared to the 6T SRAM [3].

In hold mode, both RWL and WL are turned off, isolating the storage nodes from external connections. The cross-coupled inverters provide stable positive feedback to retain the stored data, even over extended

periods [4]. This isolation reduces power wastage, making the 8T SRAM more energy-efficient than the 6T SRAM, especially in low-power designs [5]. The 8T SRAM offers several benefits over the 6T design, including enhanced read stability due to the isolated read path, reduced bit-line disturbances, and improved power efficiency and performance [7]. Additionally, the 8T SRAM performs better at lower supply voltages, making it an excellent choice for energy-efficient systems [9]. These improvements make the 8T SRAM a strong candidate for low-power, high-performance VLSI applications, delivering both power savings and operational reliability.

8T SRAM CELL WITH POWER GATING :

The 8T Static Random Access Memory (SRAM) cell with power gating is a dedicated design with the aim of reducing power consumption while maintaining the enhanced read stability of the 8T structure, particularly at technology nodes greater than 90nm. The traditional 6T SRAM cell, as discussed in the literature, consists of two cross-coupled inverters and two access transistors with read, write, and hold modes, but is afflicted with the issue of high leakage power in standby mode due to scaling-induced short-channel effects [1]. The 8T SRAM cell enhances the read stability issue of the 6T design by incorporating two additional transistors to create a dedicated read path, separating the read and write operations, which improves stability and is suitable for low-power applications [2]. Leakage power remains an issue during standby mode. In an effort to address this, power gating is incorporated in the 8T SRAM design by adding a footer transistor to disconnect the cell from the ground during idle time, lowering static power dissipation significantly, as discussed in the case of 6T SRAM with power gating [7]. The design and operation of the power-gated 8T SRAM cell are explained in this section, supplemented by its schematic.

The power-gated 8T SRAM cell schematic in Figure 4 shows the incorporation of power gating into the 8T architecture. The fundamental storage element is two cross-coupled inverters built by PMOS transistors P1 and P2 (pull-up) and NMOS transistors N1 and N2 (pull-down), between supply voltage (VDD) and ground (GND), that store complementary data at nodes Q and QB [1]. N3 and N4 are the write access transistors, driven by the word line (WL), between Q and the bit line (BL) and QB and the complementary bit line (BLB) for writing. The 8T SRAM's dedicated read path is NMOS transistors N5 and N6, driven by the read word line (RWL) and the stored value at Q, respectively, with the read bit line (RBL) as the output [2]. Even though the schematic does not schematically show the power gating transistor, the literature shows that the addition of a footer NMOS transistor between the pull-down NMOS transistors (N1, N2) and GND is the method of adding power gating in power-gated SRAM designs [7]. The footer transistor, driven by a power gating signal (PG), isolates the cell from GND in standby mode, minimizing leakage currents and static power dissipation, an approach that can be applied to the 8T SRAM to realize similar power savings.

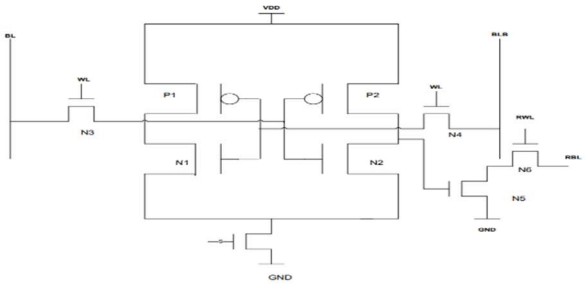

Fig 4: 8T SRAM CELL WITH POWER GATING

The operation of the power-gated 8T SRAM cell involves three primary modes—write, read, and hold—

with power gating activated during idle periods to minimize power consumption. During a write operation, the WL is set high, enabling N3 and N4 to transfer data from BL and BLB to the storage nodes Q and QB, overwriting the existing values, while the power gating transistor remains on to keep the cell powered [3]. For a read operation, RWL is activated, turning on N5, and RBL, precharged to VDD, either discharges through N5 and N6 (if Q = 1) or remains high (if Q = 0), allowing the data to be sensed without disturbing the storage nodes, thus ensuring read stability [2]. In hold mode, both WL and RWL are low, isolating the cell from the bit lines, and the cross-coupled inverters maintain the stored data. When the cell is idle, the power gating signal turns off the footer transistor, disconnecting the pull-down path to GND, which minimizes leakage currents, as described in the literature for power-gated SRAM designs [7]. This approach effectively reduces static power dissipation, though it introduces a wake-up delay when the cell transitions from standby to active mode, a trade-off noted in the document [5].

The power-gated 8T SRAM cell offers significant advantages for low-power memory applications, combining the read stability of the 8T architecture with the power-saving benefits of power gating. The dedicated read path, formed by N5 and N6, ensures that read operations do not interfere with the storage nodes, making the cell more reliable at lower supply voltages, a critical feature for energy-efficient systems [2]. The addition of power gating addresses the leakage power issue, which is a major concern in 90nm technology, by isolating the cell during standby mode, as demonstrated in the context of 6T SRAM with power gating [7]. However, the wake-up delay introduced by power gating, as the cell transitions from standby to active mode, must be carefully managed to avoid performance degradation, a challenge highlighted in the literature [5].

The schematic in Figure 4 effectively captures the structural enhancements of the power-gated 8T SRAM, illustrating the roles of the write access transistors (N3, N4), the read path transistors (N5, N6), and the control lines (WL, RWL) in achieving a balance between power efficiency and performance, making this design a promising candidate for low-power VLSI systems.

SIMULATION RESULTS:

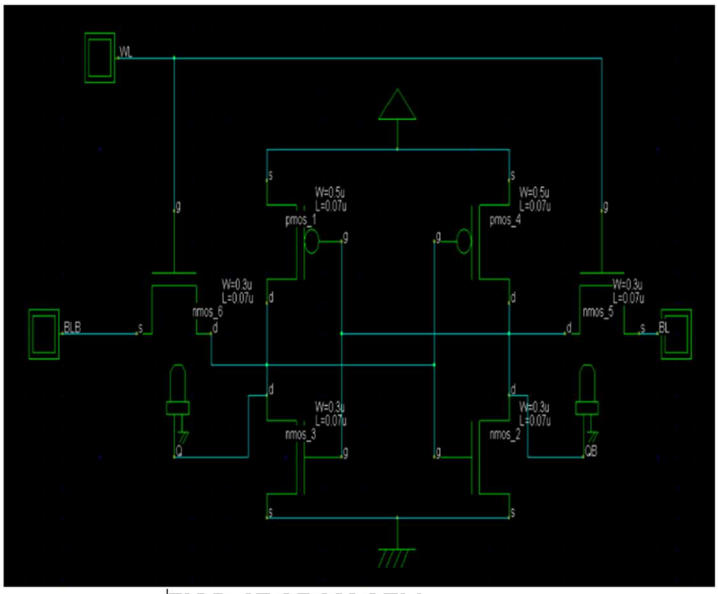

FIG5: 6T SRAM CELL

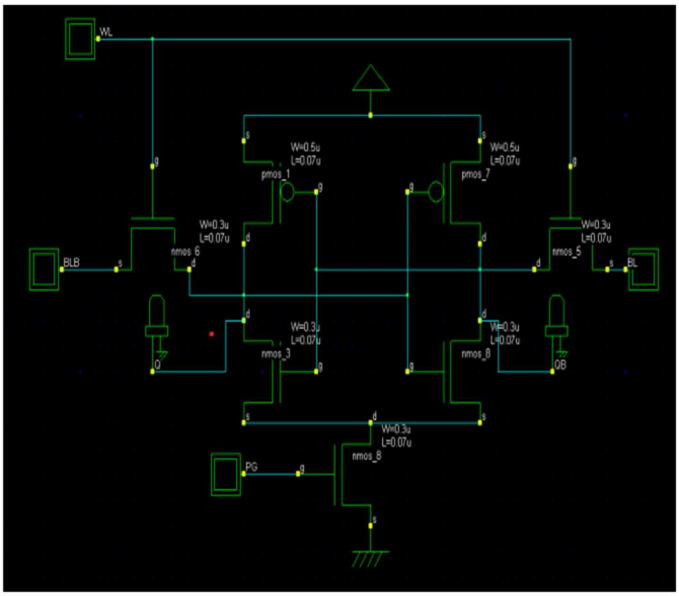

FIG 6: 6T SRAM WITH POWER GATING

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Volume : 54, Issue 4, No.1, April : 2025

FIG7: Output wave form of 6T SRAM cell

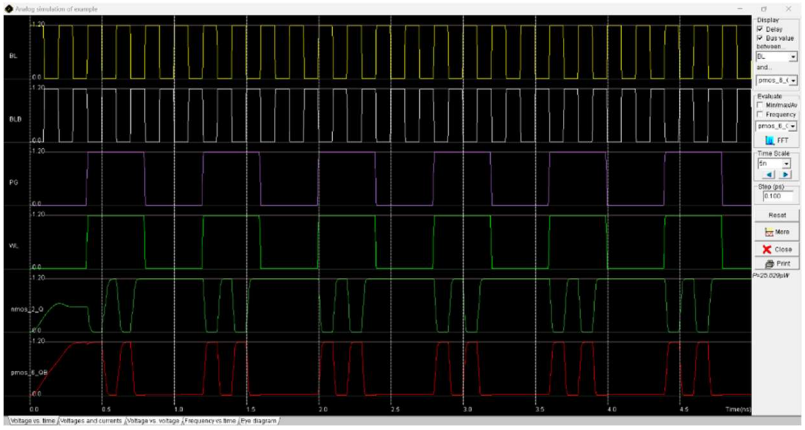

FIG 8: OUTPUT WAVEFORM OF 6T SRAM WITH POWER GATING

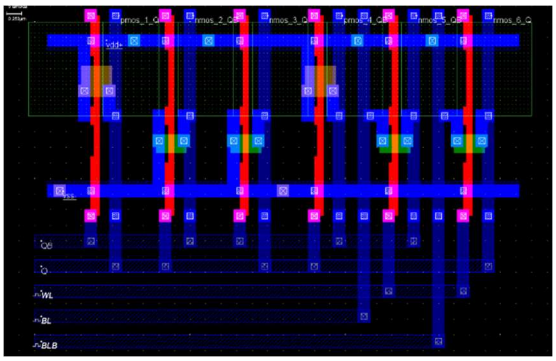

FIG 9: 6T SRAM CELL GATING STICK DIAGRAM

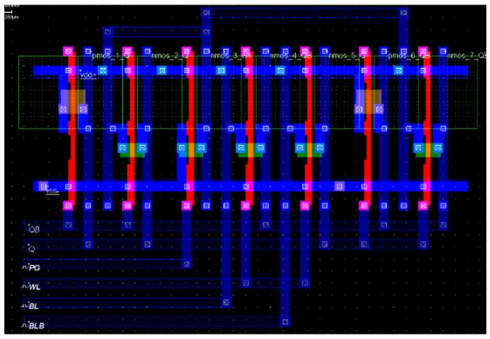

FIG 10: 6T SRAM CELL WITH POWER

6T SRAM CELL			6T SRAM CELL WITH POWER GATING		
Vdd(V)	Power Consumption(mw)	Delay(ps)	Vdd(V)	Power Consumption(mw)	Delay(ps)
1.2V	0.028	120	1.2V	0.025	138
2V	0.259	100	2V	0.231	115
3V	2.757	85	3V	0.293	98
4V	3.606	70	4V	0.570	81

Table 1: Comparison of 6T SRAM CELL AND 6T SRAM CELL WITH POWER GATING

The simulation outputs for the 6T SRAM cell with and without power gating in 90nm CMOS technology

Industrial Engineering Journal
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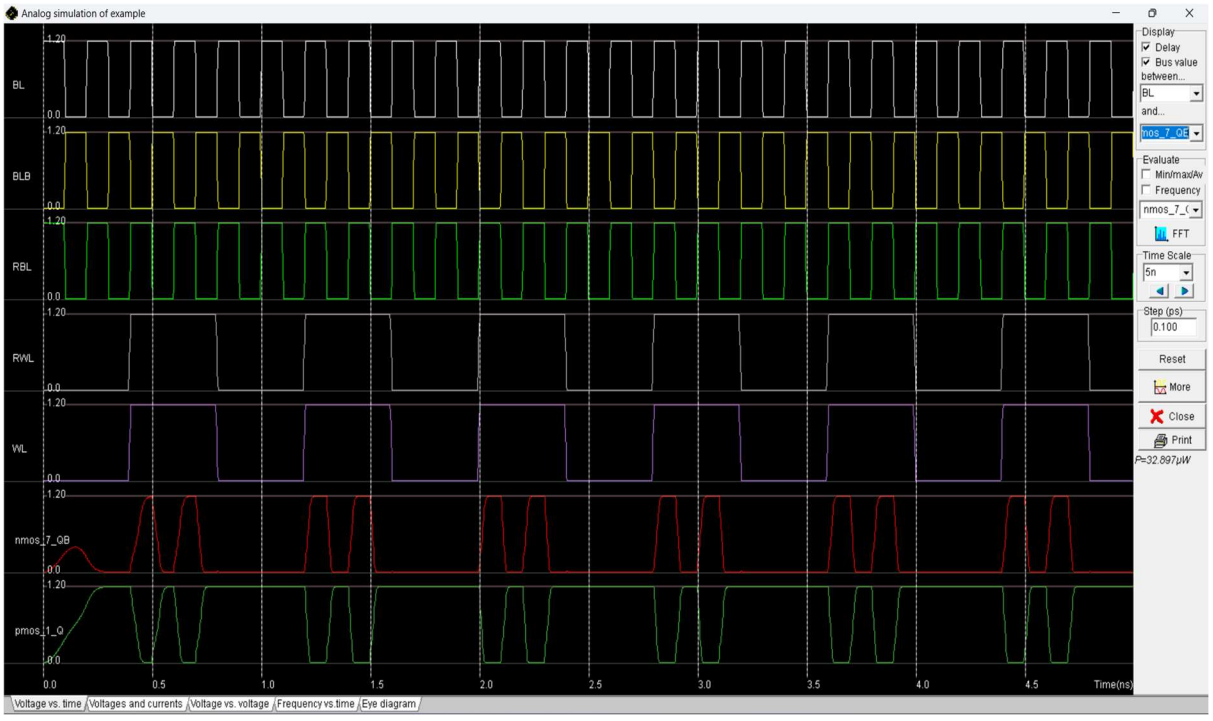
Volume : 54, Issue 4, No.1, April : 2025

identify the efficiency of power gating in minimizing power consumption at the expense of adding a trade-off in read delay as listed in Table 1. Figure 5 shows the traditional 6T SRAM cell, which is made up of two cross-coupled inverters and two access transistors and represents the central structure for storing and accessing data . Figure 6 illustrates the power gated 6T SRAM where a footer NMOStransistor is inserted between ground and the pull-down NMOS transistors, driven by a power gating signal to reduce leakage power in standby mode . The stick diagrams in Figure 6 (6T SRAM Stick Diagram) and Figure 10 (6T SRAM with Power Gating Stick Diagram) present the layout-level structure, illustrating the transistor placement and the extra footer transistor in the power-gated design, adhering to 90nm technology layouts [15]. The 6T SRAM cell output waveform, presented in Figure 7, illustrates voltage levels of the bit lines (BL, BLB), word line (WL), and storage nodes (Q, QB) during read, write, and hold operations, validating the functionality of the cell in all modes. precharging of bit-line, and sensing of data, which are essential for calculating the read delay. Figure 8 (Output Waveform of 6T SRAM with Power Gating) includes the power gating signal (PG) for the power-gated 6T SRAM, which is high in active mode and low in standby mode, thus reducing leakage power.

given for the 6T SRAM with power gating at 1.2 V indicates a read delay of 140 ps, which is the time from the WL rising edge to the bit-line voltage falling to 50% of Vdd, consistent with the reported value of 138 ps in Table 1 . At 1.2 V, power consumption drops from 0.028 mW in the non-power-gated one to 0.025 mW in the power-gated one, a saving of 10.7%, proving the effectiveness of power gating in curbing static power dissipation . This is sustained at 2 V, with power consumption decreasing from 0.259 mW to 0.231 mW, a decrease of 10.8%, and at higher voltages, although 3 V and 4 V are not feasible for 90nm technology because of reliability issues . But read delay is 15% higher at 1.2 V (from 120 ps to 138 ps) and 15% higher at 2 V (from 100 ps to 115 ps), which indicates the extra resistance of the footer transistor and the wake-up delay in the changeover from active mode to standby mode . These findings verify that power gating reduces power consumption in the 6T SRAM considerably, and it is appropriate for low-power designs, although the increased read delay needs to be taken into account in performance-critical systems .



Industrial Engineering Journal
ISSN: 0970-2555
Volume : 54, Issue 4, No.1, April : 2025

FIG13: OUTPUT WAVEFORM OF 8T SRAM CELL

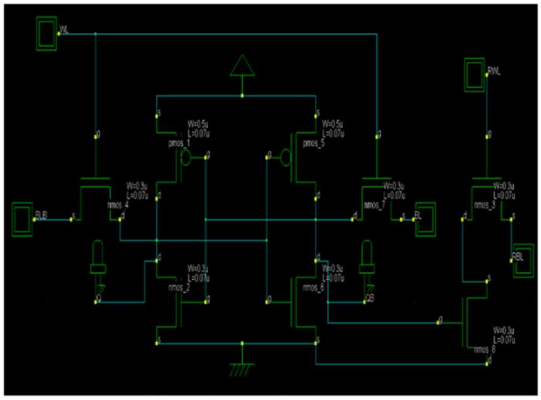


FIG 11:8T SRAM CELL

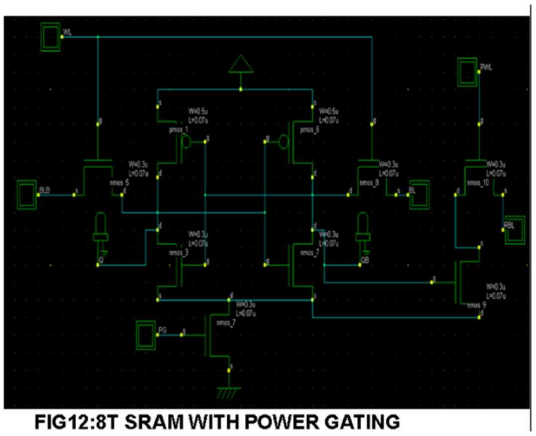


FIG12:8T SRAM WITH POWER GATING

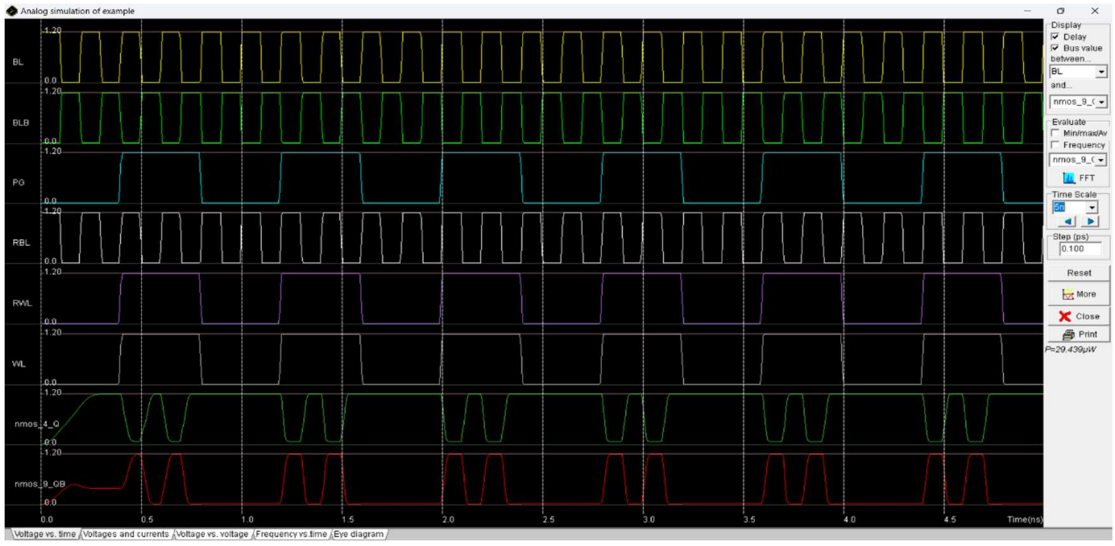


FIG 14: OUTPUT WAVE FORM OF 8T SRAM WITH POWER GATING

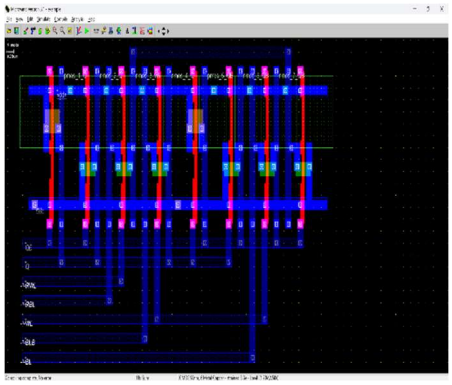


FIG 15:8T SRAM STICK DIAGRAM
STICK DIAGRAM

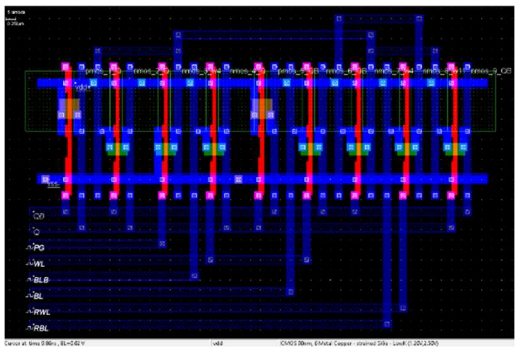


FIG 16: 8T SRAM WITH POWE GATING

TABLE 2: Comparison of 8T SRAM CELL AND 8T SRAM CELL WITH

8T SRAM CELL			8T SRAM CELL WITH POWER GATING		
VDD (V)	**Power Consumption(mw)**	**Delay(ps)**	**VDD(V)**	**Power Consumption(mw)**	**Delay(ps)**
1.2V	**0.032**	**97**	**1.2**	**0.028**	**150**
2V	**0.297**	**82**	**2V**	**0.268**	**128**
3V	**2.753**	**70**	**3V**	**0.411**	**109**
4V	**3.606**	**60**	**4V**	**1.158**	**93**

POWER GATING:

The simulation outcomes of the 8T SRAM cell, with and without power gating in 90nm CMOS technology, highlight the advantages of power gating in limiting power consumption as well as the better read stability of the 8T SRAM, though with increased read delay, as given in Table 2. Figure 11 depicts the 8T SRAM cell, which extends the 6T concept by introducing two extra transistors to create a dedicated read path, regulated by a read word line (RWL) and read bit line (RBL), improving read stability by decoupling read and write operations. Figure 12 illustrates the 8T SRAM with power gating, featuring a footer transistor to minimize leakage power, just like the 6T structure . The stick diagrams in Figure 15 (8T SRAM Stick Diagram) and Figure 16 (8T SRAM with Power Gating Stick Diagram) illustrate the layout, pointing out the extra read path transistors and the power gating transistor, presenting a clear structural perspective in the 90nm technology node . The 8T SRAM cell output waveform, presented in Figure 13, consists of signals like BL, BLB, RBL, RWL, WL, and storage nodes (Q, QB), exhibiting steady operation in read, write, and hold modes, with the special read path guaranteeing little disturbance to the storage nodes [8]. Figure 14 (Power Gating Waveform of 8T SRAM) contains the power gating signal (PG), which is active in active operations to keep the cell powered and reduce leakage during standby. The waveform earlier shown for the 8T SRAM with power gating at 1.2 V exhibits a read delay of 150 ps, taken as the time from the RWL rising edge to the RBL falling to 50% of Vdd, which represents the effect of the extra transistors and power gating [5]. At 1.2 V, the power consumption reduces from 0.032 mW in the non-power-gated to 0.028 mW in the power-gated design, a reduction of 12.5%, validating the efficacy of power gating in lowering static power dissipation .

This trend continues at 2 V, with power consumption decreasing from 0.297 mW to 0.268 mW, a reduction of 9.8%, and at increased voltages, although 3 V and 4 V are not viable for 90nm technology [15]. The read delay of the non-power-gated 8T SRAM is 97 ps at 1.2 V, but rises to 150 ps with power gating, a 54.6% increase, owing to the exclusive read path and wake-up delay caused by power gating . The 8T SRAM with power gating provides better read stability and is more suitable for low-voltage applications such as IoT and mobile, where the 6T SRAM can suffer from read failures due to poor noise margins The findings confirm that the 8T SRAM with power gating provides substantial power reduction while maintaining improved stability and is a potential solution for low-power memory design This study of the design and power analysis performance of SRAM with power gating by 90nm technology has effectively

proven the efficiency of power gating in cutting down power consumption for both 6T and 8T SRAM cells, solving the fundamental challenge of leakage power in new low-power VLSI systems. The application of power gating in the designs greatly reduces static power dissipation by disconnecting the cells from the ground when in standby mode, realizing power reductions like from 0.028 mW to 0.025 mW for the 6T SRAM and from 0.032 mW to 0.028 mW for the 8T SRAM at 1.2 V [Table2]. But the 8T SRAM with power gating has notable advantages over 6T SRAM with power gating, most notably in read stability, with its dedicated read path created by two extra transistors decoupling the read and write operations and excluding disturbance of storage nodes—a prevailing problem in 6T SRAM cells for smaller technology nodes . Simulation outcome confirms that the power-gated 8T SRAM operates steadily through write, read, and hold modes with a read delay of 150 ps at 1.2 V against 140 ps for the power-gating enabled 6T SRAM while realizing substantial power savings, supporting the promise of power gating for power-efficient memory design .

CONCLUSION :

The comparative comparison of the power gating 6T and 8T SRAM cells sheds light on power reduction vs. performance trade-off. The 8T SRAM with power gating shows a little bit more read delay (e.g., 150 ps compared to 140 ps at 1.2 V) because of the extra transistors but is compensated for by its increased read stability and thus is more suitable for low-voltage designs like battery-driven devices and IoT systems . 8T SRAM power gating is the better solution for high-density memory applications, with the best power efficiency, stability, and performance, as attested by available research . This work supports the creation of power-efficient SRAM designs in order to meet the serious power limitations in contemporary VLSI systems. Future research may consider reducing the wake-up delay through more sophisticated approaches such as MTCMOS designs and investigation of power-gating integration with other low-power techniques to better optimize the effectiveness of 8T SRAM cells in next-generation VLSI systems .

The comparative analysis between power-gated and non-power-gated 6T and 8T SRAM cells highlights the trade-offs between power reduction and performance, particularly the wake-up delay introduced by power gating. While this slightly impacts access time, it is outweighed by substantial power savings, making power-gated SRAM an optimal choice for low-power applications . The 8T SRAM with power gating emerges as a promising solution for high-density memory applications, offering an optimal balance of power efficiency, stability, and performance, as emphasized in existing studies .

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