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LOW POWER HIGH SPEED DESIGN OF N-BIT DIGITAL COMPARATOR AT 16NM VLSI REGIME

V. Satyavathi Pg Student Dept. of ECE Lendi Institute of Engineering and Technology, Jonnada (village), Vizianagaram (Dist), India Email: satyakethaki29@gmail.com
B. Sridhar Professor Dept. of ECE Lendi Institute of Engineering and Technology, Jonnada(village), Vizianagaram (Dist), India Email: srib105@gmail.com

ABSTRACT
Designing a digital comparator with N bits as inputs plays an important role in VLSI. The proposed method plays an important role in computing N-bit comparator circuit behavior. It will consume less power, and the area requirement is also less. In all arithmetic operations, comparison is the most basic method. In the proposed method, comparison will begin with the least significant bit and continue up to the most significant bit. It means bit-wise operations start from the least significant bit to the most significant bit, etc. The proposed method mainly contains two blocks. The first block is a comparison node, and the second block is an observation node. In the comparison node, all the inputs are compared bit-wise, from least significant bit to most significant bit. In comparison to two bits, the role of XOR gates is vital. The power dissipation becomes less 02.87.nano watts. , delay becomes less 40.02nano seconds. Delay reduced by 50%.The proposed method uses a low-cost XOR gate with only six transistors. This method consumes only 0.8 VDD as a supply voltage, and the proposed comparator block consumes less power and high speed too. The entire proposed method was designed and validated using Mentor Tanner 16nm Technology.

Keywords:
N-Bit Digital Comparator, Low power, High Speed, CMOS XNOR.

I.INTRODUCTION
The need of comparators are vital in so many circuits, especially in Analog to digital converters , in ADC's[1] the role of comparators is used to compare the magnitudes of the two inputs. In general comparators are designed by operational amplifier. Comparators are designed by Dynamic transistors also. The role of transmission gates play an a important role in designing the comparators. There are two counted binary numbers that are compared based on their magnitude[2]. There are some chances in the data may be or may not be them can be higher, lower, may be other than two quality to the other number. Its comparison is made by using Design , so it is known as a comparison method. As we know, in many basic design elements, the application we use is the digital comparator, which helps in comparing the activity of the output as a part of it. The final output is based on the digital comparator, and the result is obtained accordingly. The following are the applications that are spread in different fields: digital images also can be comprised by converting the images in tp pixels then into digital values and then comparison is made as per the digital bits. In previous methods designed by 180nm Technology[4]. With 180nm technology the area required on silicon becomes more. Not only area power dissipation also becomes more.

II.LITERATURE SURVEY
The basic building blocks of a digital comparator are the same as the applications mentioned above. For better optimization of the comparator design, the main component used is the general purpose, which is a computer architecture where we need to improve the memory addressing [5] logic. The large usage of the comparator logic is based on their different designs, which help in computation based on their call reduction in size and power optimization in area and dealy.in which they consist of 2-bit comparators. In the proposed method 16nm Technology is used. So area becomes less on

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silicon[8]. Not only area power consumption becomes very less, the power[9] supply around 0nly 0.8 VDC[10].

III.EXISTING METHOD

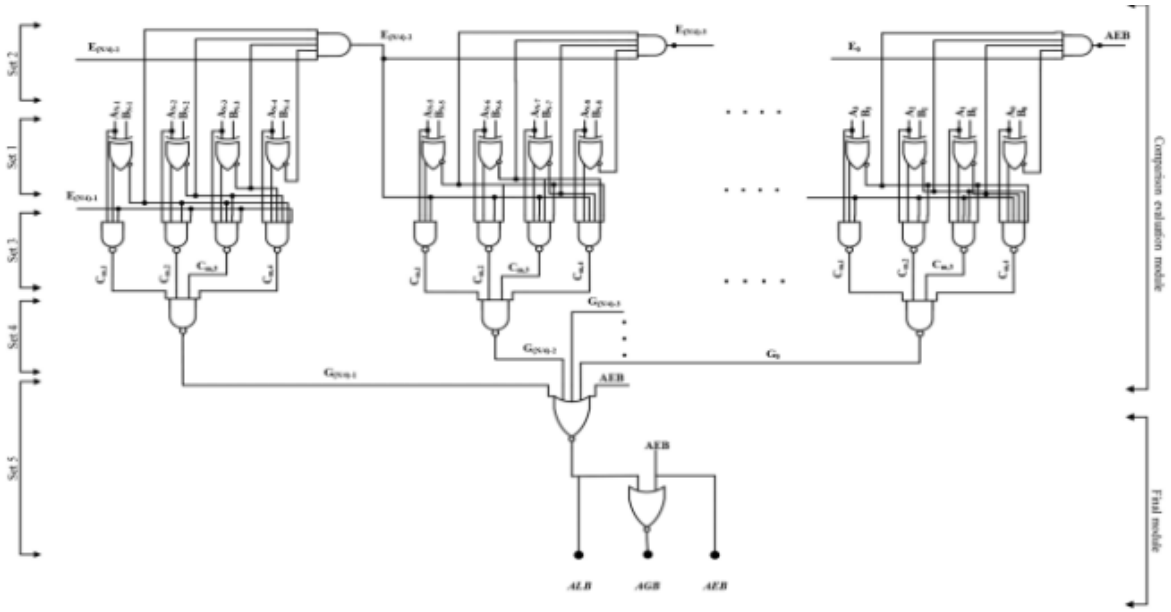

Fig 1: Existing scalable method 4 bit comparator

In existing scalable comparator takes more number of transistors to evaluate the performance of 4 bit comparator[1]. With the existing method the power requirement is going to increase much, and also average power, maximum power and dynamic power consumption also increased a lot. In existing method more number of transistors are required in designing of XOR-XNOR cell, [12] to design single XOR cell 12 Transistors are required, for XNOR also 12 Transistors are[13] required. With this more are is going to occupied in silicon.

In existing method the number of transistors are as follows 1- 3 input NAND -6T= 6 transistor,1-4 input NAND-8T= 8 Transistor ,1-5 input NAND-10T= 10 Transistor ,1-6 input NAND -12T=12T Transistor ,2-2 input NOR – 4T*2=8T Transistor,1- 5 input AND = 13 Transistor,2 input XOR-XNOR-14T*4=56 Transistor, total 113T transistor. In existing method the supply voltage around 1.8 VDC. The power dissipation becomes more. 121.97 [14], delay becomes [140.73], the power dissipation becomes more. 58.97 [15], delay becomes [70.73], the power dissipation becomes more. 97.68 [16], delay becomes [112.54]

IV.PROPOSED METHOD

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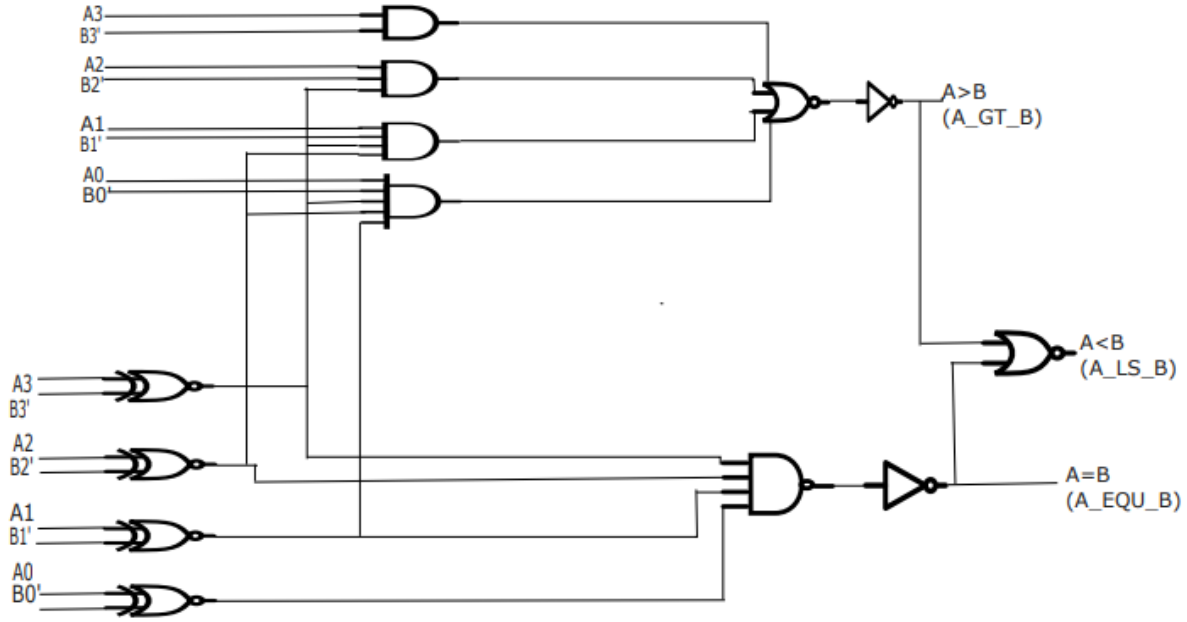

Fig 2: Proposed method with XNOR based 4 bit comparator

The above proposed schematic contains 4 inputs in which inputs are varied from A0-A4 and B0-B4. It contains three outs they are A>B, A<B and A=B.

V.PROPOSED XNOR GATE

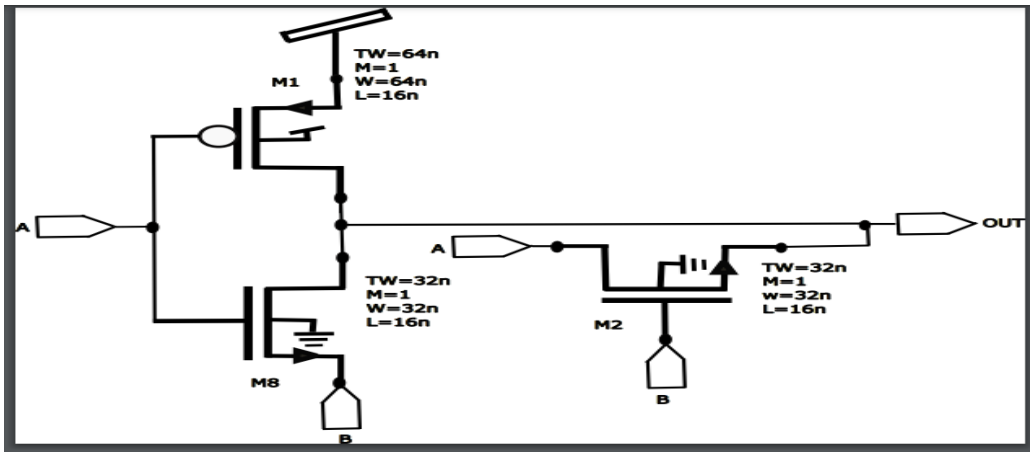

Fig 3: Proposed method with XNOR circuit with 3 transistors.

The above schematic contains three transistors to implement the behavior of XOR gates. It contains one PMOS Transistor and two NMOS Transistors. The working principle of above schematic as if A input is 0 B input 0, Output is 1. If a input is 1 B input 1, Output is 1. If an input is 1 B input 0, Output is 0. if A input is 0 B input 1, Output is 0. In existing method more number of transistors are required in designing of XOR-XNOR cell [17], to design single XOR cell 12 Transistors are required, for XNOR also 12 Transistors are required. With this more are is going to occupied in silicon. To avoid more area we are going to design proposed method with only 3 Transistors only to design XNOR circuit. With the proposed method the power consumption and area requirement is going to decrease a lot. Performance of the circuit is gonging to increase a lot.

VI.OPERATION OF THE 4 BIT COMPARATOR

To produce A>B , the following components play an important role they are one inverter, four input NOR gate . S1 is the output of a two input AND gate, S1 is the output of AND gate and A3 and B3 complement. S2 is produced by the three input AND gate, A2, Complement of B2 and Third input from XOR gate output that is S5. S3 Produced by 4 input AND gate the inputs are A1, complement of

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B1, S5, and S6. S4 Produced by 5 input AND gates the inputs areA0, complement of B0, S5, S6 and S7. To produce A<B the role of A>B and A=B is very important. To produce A<B we used XNOR gate. The inputs to the XNOR gates are output of the A=B,and A>B. To produce A=B output the role of S5, S6, S7, S8 is very important. All these S5, S6, S7 and S8 are given to the NAND gate, NAND gate produced output, that's output is given to the inverter. The last stage of the A=B is the output of the inverter. G1 is the XOR gate which is produce the output S5, A3, B3 are the inputs to the G1 XOR gate. G2 is the XOR gate which is produce the output S6, A2, B2 are the inputs to the G1 XOR gate. G3 is the XOR gate which is produce the output S7, A1, B1 are the inputs to the G1 XOR gate. G4 is the XOR gate which is produce the output S5, A0, B0 are the inputs to the G1 XOR gate.

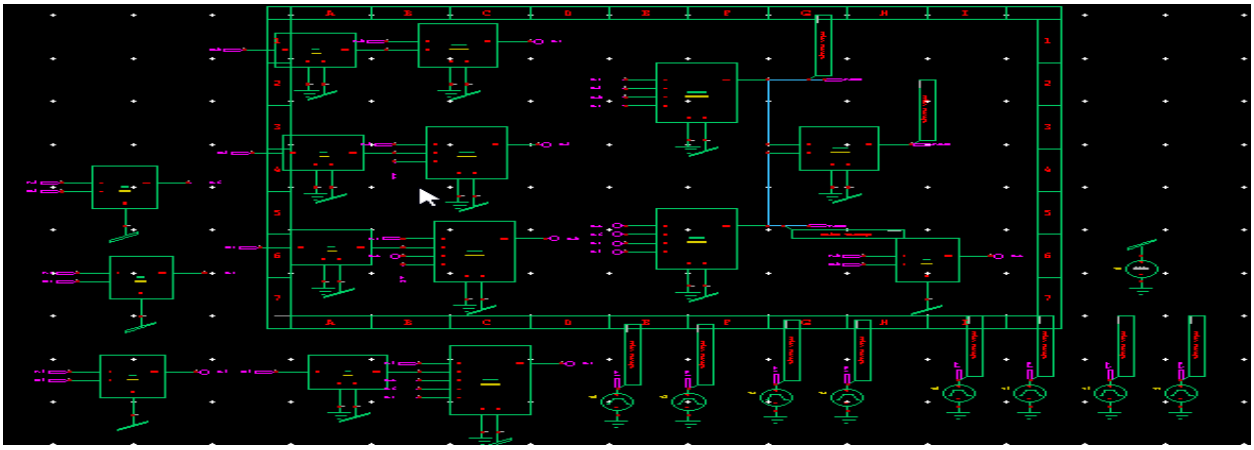


Fig 4: Proposed method with XNOR based 4 bit comparator

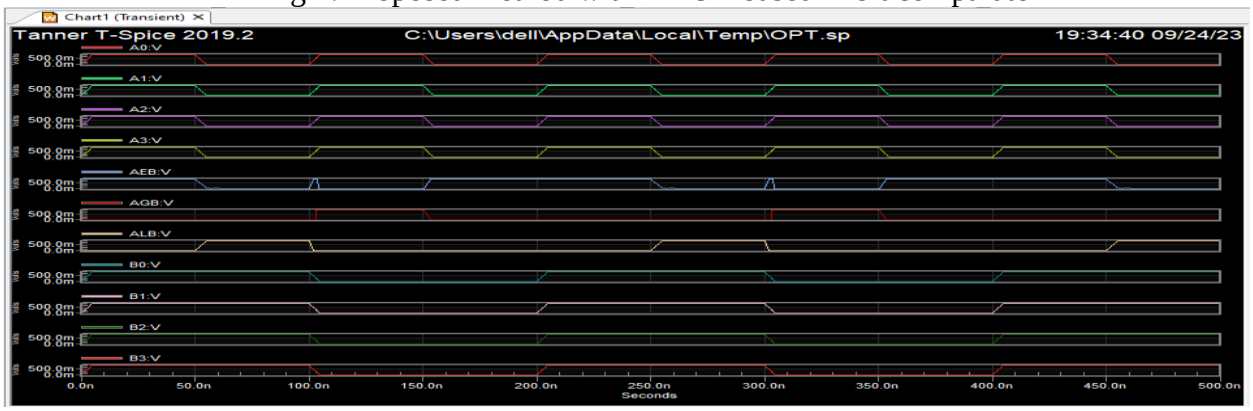
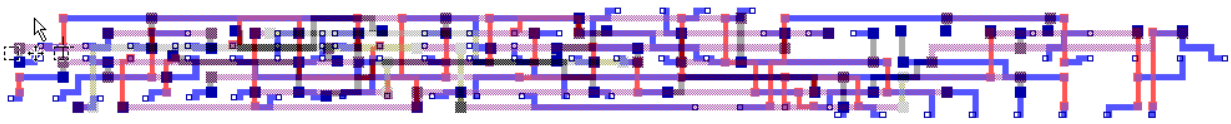


Fig 4:simulation Proposed method with XNOR based 4 bit comparator

The above figure shows the simulation of the 4 BIT digital comparator. To validate the behavior[18] of the above schematic Tanner 16nm Technology has been used. The number of transistors required for the proposed method as follows.

In Proposed method the number of transistors are as follows XNOR-3T*4=12Transistor,Inverter [19] 2T*4=8Transistor,2 input AND 1*6T=6Transistor,3 input AND 1*8T=8Transistor,4 input AND =10Transistor,5 input AND =12T transistor,4 input AND =10Transistor,4 input OR = 10 Transistor,2 input NOR =4 Transistor, Total number of transistors are 80Transistor.

VII LAYOUT OF PROPOSED METHOD



Layout Verses Schematic

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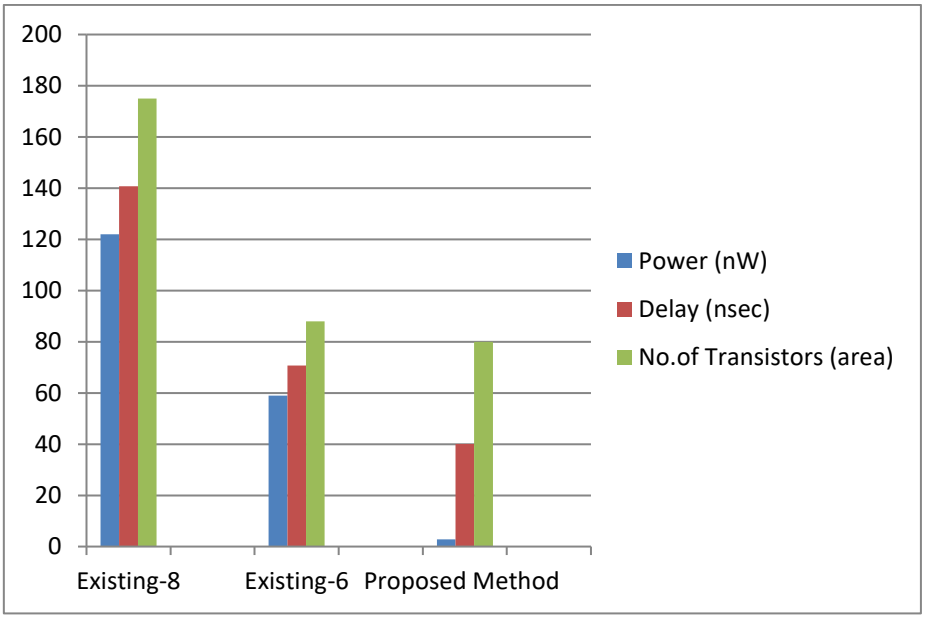
To draw the layout, the basic rules are as follows: to draw the layout of PMOS, to draw the gate, use polysilicon that's red; for the drain and source, brown is used. To draw the layout of NMOS[20] , to draw the gate, use polysilicon, whish's red; for the drain and source, green color is used. For making wiring connections between transistors, metal 1 is used; for metal drawing in layout, blue is used.

VIII.COMPARISON TABLE

S.NO	Method	Power (nW)	Delay (nsec)	No.of Transistors (area)
1	Existing Method [8]	121.97	140.73	175
2	Existing Method [6]	58.97	70.73	88
3	Existing method	97.68	112.54	113
2	Proposed Method [3]	02.87	40.02	80



IX CONCLUSION

To design a digital comparator with N Bits as a inputs play an important role in VLSI. The proposed method plays an important role in computing N Bit comparator circuit behavior. It will consume less power and area requirement is also less. In all arithmetic operations comparison is of two digital bits magnitude is most basic method. In proposed method comparison will begin with least significant bit and continuous up to most significant bit. It means bit wise operations starts from least significant bit to most significant bit etc. the proposed method mainly contains two blocks first block is comparison node and second block is observation node. In comparison node all the inputs are compared bit wise from least significant bit most significant bit.in comparison of two bits the role XOR gates is vital, In the proposed method designed low are XOR gate, which comprised only 6 transistors. This method consumes only 0.8VDD as a supply voltage, with this proposed comparator block consumes less power and high speed too. The entire proposed method designed and validated using Mentor Tanner 16nm Technology.

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