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REALIZATION OF HIGH PERFORMANCE AND POWER OPTIMIZED SCHMITT TRIGGER BASED 9T SRAM AT 16NM CMOS TECHNOLOGY

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ABSTRACT
This paper presents a one-sided Schmitt-triggerbased 9T static random access memory cell with low energy consumption and high read stability, write ability, and hold stability yields in a bit-interleaving structure without write-back scheme. The proposed Schmitt-trigger-based 9T static random access memory cell obtains a high read stability yield by using a one-sided Schmitt-trigger inverter with a single bit-line structure. In addition, the write ability yield is improved by applying selective power gating and a Schmitt-trigger inverter write assist technique that controls the trip voltage of the Schmitt-trigger inverter. The proposed Schmitt-trigger-based 9T static random access memory cell has 0.79, 0.77, and 0.79 times the area, and consumes 0.31, 0.68, and 0.90 times the energy of Chang's 10T, the Schmitt-trigger-based 10T, and MH's 9T static random access memory cells, respectively, based on 45-nm CMOS technology

Keywords : 9T static random access memory cell, one-sided Schmitt-trigger inverterand CMOS technology.

1.INTRODUCTION
Since For system-on-chips (SoCs) that run on limited battery or harvested energy, and energy collecting devicesminimising power consumption has become increasingly important. Since consumes a substantial portion of the available space. SoC's real estate [1], cutting down on its power consumption is crucial for bringing the SoC's total power usage down.Effectively, strength consumption can be lowered by decreasing the supply voltage (VDD). When the power goes off in a quadratic fashion when the VDD scales down [2]. Yet, operational yields decrease and delay and soft error rates (SERs) rise as VDD grows down. Under threshold voltage (Vth) The delay increases exponentially in the region where VDD is less than Vth. Even when very low power is attained, the energy consumption rises as a result of the greatly higher static energy consumption. When compared to super-Vth operation, operating in the near-Vth zone, where VDD is just above Vth, can significantly reduce electricity, and vastly reduce the delay compared to sub-Vth operation. Hence, (static random access memory) consumes a substantial portion of the available space.Vth region to lessen energy consumption [3]. The -particle-induced soft

error becomes significant in near-Vth operation [4, 5]. It's because the reduced SER is producing a larger charge while in operation around the Vth [6]. As non-bit-interleaving structures store words' bits in order, it is possible for multiple bits to go wrong in a single word. This is due to the fact that When a soft mistake occurs, neighbouring cells concurrently experience bit errors. Error correction code (ECC) circuits are large and power-hungry because of the need to fix errors in multiple bits. Nonetheless, bit-errors are still possible because to the spatial interleaving of the bits that make up each word. occur in each and every one of them in a bit-interleaving structure. A basic error correction code (ECC) circuit may rectify errors involving a single bit [7]. Hence, the bit-interleaving structure has been used in the near-Vth region to address the rising SER. At voltages near the threshold, the transistor current is extremely sensitive to minor variations in Vth. Specifically, SRAM cells are susceptible to Vth fluctuation because they require incredibly small transistors to achieve a high density in a given area. limited area Additionally, since With conventional 6T SRAM cells, read stability and write ability are reduced, making it difficult to achieve steadiness in reading and the ability to write at the same time that is adequate. There have been many different designs for SRAM cells [5, 7]-[11] proposed in order to provide enough read stability and write capability in the neighbourhood of Vth. These memories have a number of limitations, including a high power consumption, an unnecessary huge SRAM cell size, and inadequate write-back support for bit-interleaving architectures. having the following characteristics: a bit-interleaving structure that does not have a write-back mechanism.Both selective power gating and ST inverter writing are included. aid technology enhance write performance while minimising energy consumption and footprint thanks to a BL topology. The inverter's cross-coupled design between the traditional and Schmitt-trigger (ST) types improves read stability.

2.LITERATURE SURVEY

Sub-threshold Static Random Access Memory (SRAM) Implemented in 65 nm CMOS: Variation in the Static Noise Margin .As the importance of doing so in memory design develops, it is becoming increasingly customary to run memories on reduced supply voltages. Current research on sub-threshold logical operations implies that operations using the least amount of energy are viable in this particular setting. These two advancements imply that there is a point of equivalence in applications that are energy-constrained and run on SRAM. at appropriate subthreshold levels for the circuitry. At sub-threshold voltages, it is more difficult to obtain significant static noise margins (SNM); therefore, it is crucial to comprehend how your actions will influence the final outcome. Due to its impact on size, DD, temperature, and local and global threshold shift, a 65-nm process requires SNM for sub-threshold bitcells. The focal point of this painting. We present a method for estimating SNM in the worst-case situation due to the fact that it is near the end of the distribution. fact that variety has an outsized influence on SNM. The creation of subthreshold digital circuits has recently emerged as a potential low-energy alternative for use in applications that require a lot of power. Logic circuits have been the primary focus of the vast bulk of sub-threshold design research (e.g., [1]). SRAMs are the primary memory used by a few digital processors [2, 3], despite the fact that they take up an excessive amount of

space and need an excessive amount of power. Capacitances of switching that are high in both the bitlines and the wordlines may account for the majority of the chip's overall leakage, resulting in energy-intensive SRAM accesses. To reduce leakage power and access energy, SRAMs can be designed to operate in the subthreshold range. Moreover, SRAM must be combinational logic compatible with voltages below the system integration barrier. Some modern low power memory systems run at subthreshold voltages (e.g., [4]). Sub-threshold storage modes and SRAMs that work with logic below the threshold are becoming a reality as the industry grows. While information is being saved in a bitcell, the wordline is pulled low, which causes the nMOS access transistors to become inoperable. The data that is stored by back-to-back inverters must have bi-stable functioning points in order to maintain its authenticity over the long term. The bitcell's static noise margin, also known as the SNM, is the parameter that most accurately represents the rate at which these inverters can keep their state [5]. It is possible to apply noise originating from the SNM voltage source to the outputs of the two inverters without having an effect on the cell's ability to transmit data in a reliable manner. When SNM is applied to a bitcell, a bitcell will become:, It determines the voltage noise needed at bitcell nodes to flip a bit. For the purpose of modelling SNM, the conceptual framework that is illustrated in Figure 1 [5] is supplied. Each node that is part of a bitcell serves as a potential entrance point for a new noise source, and some of these noise sources may have monetary value. When the concentration increases, there is a change in the cell's level of stability. The SNM is the graphical depiction of a bitcell that is used the most frequently. The results are illustrated in Figure 2. Figure 1 provides a visual representation of the voltage transfer characteristics (VTC) exhibited by inverters 1 and 2. By taking into consideration the length of the side of the square that falls within the zone where the value of increases from zero, it is plainly clear that this definition is appropriate. the length of the side of the square that falls within the zone where the value of grows from zero. As a direct consequence of this, the symbol for Inverter 1 in the illustration flips its orientation to the opposite, while the VTC symbol for Inverter 2 shifts to the right.After both curves have travelled the SNM distance, they will meet at two different places where they intersect each other. The cell would flip when it was subjected to a subsequent shock. Even if the SNM is required, active operation is more detrimental to the performance of SRAM than hold. Figure 3 shows that all of the bitlines are still precharged to the value "1."at the wordline, which signifies the start of a read access. The access transistor (,) is responsible for pulling the internal node of the due to the voltage splitting effect that occurs between it and the driving transistor. bitcell representing a zero higher (,).During the reading operation, a voltage spike causes serious damage to the SNM (read SNM). Figure 4 displays butterfly curves to indicate the drop in SNM during reading (hold and read).

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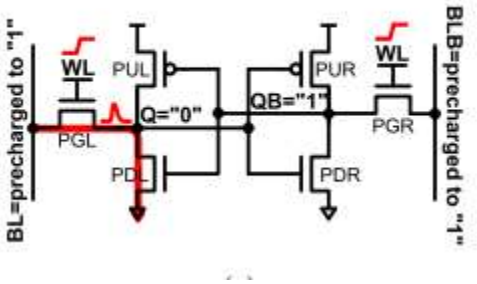

FIG.1 SRAM 6T Schematic

In Fig.1, One example of a read-disturbance cell that contains a bumped storage node is presented before us here. The ST inverter, ST 10T, and potentially ST 9T SRAM cells increase read stability. The suggested ST 9T SRAM cell outperforms cross-coupled ST inverter ST 10T SRAM cells in read reliability. These factors caused it. Read disturbance minimally activates ST 10T SRAM cell NFL. whenever node Q stores a "0.", hence decreasing PDL1 and boosting VXL. This indicates that the read disturbance will get more severe. The projected ST 9T SRAM cell, based the other hand, gets around this issue by combining ST and normal inverters in a crosscoupled topology. This is achievable because the single BL structure's storage node Q only experiences read disturbances when it is set to "0."

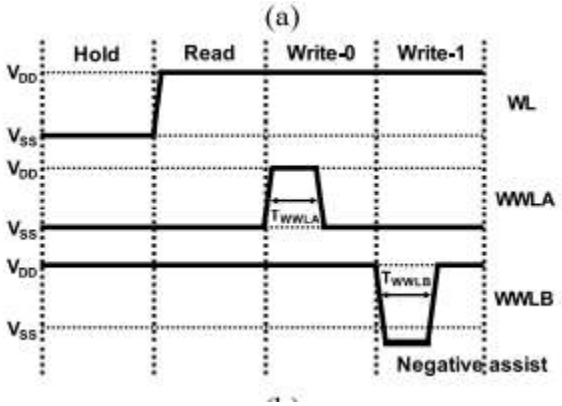

FIG 2. SRAM 6T Schematic simulation

4. PROPOSED METHOD 9T SRAM-SCHMITT TRIGGER

The plan for it An operating Figure 3 is a timing diagram for the single ST 9T SRAM cell BL configuration. The proposed ST 9T SRAM cell has a cross-coupled nMOS PG, a standard stacked-transistor inverter (PUL1, PUL2, PDL1, PDL2), and a ST inverter (PUR, PDR1, PDR2, NF). Unlike the row-based word-line (WL), the column-based WWLA and WWLB signals are printed in the same direction as the text. Two gates, PG and PUL2, are linked to WL and WWLA. WWLB is associated to the origin of NF as well as the PDL1 gate. Go to the operating room. The numbers 0 and 1 for WWLA

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and WWLB indicate the read operation, which activates PUL2 and PDL1. The central component of a battery-powered inverter. PG is triggered concurrently with WL. The BL is then either released or not, according on the information at node Q. Interference from BL is a common reason for failed reads. In the event that a read disturbance jostles the storage node and the node's voltage rises above the inverter's trip voltage, the recorded data may be inverted.The planned ST 9T SRAM cell combines conventional and ST inverters in a cross-coupled architecture to address the issue of read failure. Indicators of DC of the ST inverter are illustrated in Figures 3 and schematic, respectively. In comparison to conventional inverters, the ST inverter's trip frequency when the input voltage (Vin) changes from "0" to "1."

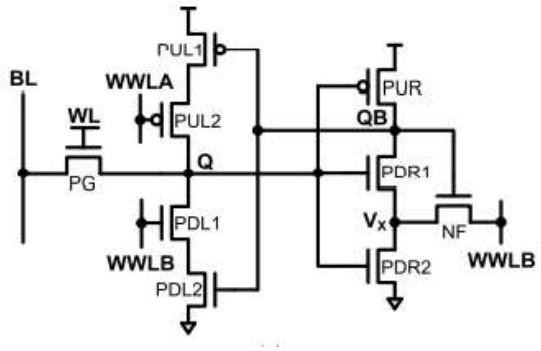

Fig 3. One sided schemit trigger schematic simulation

than the typical inverter's voltage. This is because increasing VX with The feedback transistor NF reduces PD1 strength. When compared to a normal inverter, a ST inverter is far less affected by the read disturbance that happens when the storage node is shifted by one position. Figure 4 depict the bumping storage node that is present in the read-disturbance cells . The ST inverter, together with the ST 10T SRAM cells and maybe the ST 9T SRAM cells, leads to a higher level of read stability. When compared with ST 10T SRAM cells that include cross-coupled ST inverters, the read stability of the recommended ST 9T SRAM cell is much higher. The occurrence can be attributed to these several causes. Node Q's activation of a small quantity of NFL causes an increase in VXL and a drop in the intensity of PDL1 when a "0" is stored in a ST 10T SRAM cell. As soon as the "0" is saved, this occurs. This means that the read interruption will become much more evident in the future. To solve this issue, the suggested ST 9T SRAM cell has a cross-coupled architecture, type A. This topology mixes ST inverters in place of regular inverters. Because the read disturbance only happens when storage node Q equals 0, this may be done with a single BL structure. Butterfly curves, which are generated by cells that induce a disturbance, were utilised to illustrate this idea. For reference, Figure 5 shows the read static noise margin (RSNM) for conventional 6T cells, ST 10T cells, and SRAM cells. In order to determine the RSNM, simply multiply the square's length by a constant. This RSNM was proposed. The ST 9T SRAM cell's asymmetrical construction makes it bigger when it stores a "1" than when it stores a "0," when it stays the same size. The proposed ST 9T SRAM cell accounts for the worst-case RSNM, making it comparable to other SRAM cells. The ST inverter's higher trip voltage increases the ST 10T SRAM

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cell's RSNM. The ST inverter's trip voltage is higher, explaining why. This is achieved via the suggested ST 9T SRAM cell's reduction in the amplitude of the read disturbance experienced by the ST 10T SRAM cell, hence reducing the detrimental effects of this phenomenon. highest RSNM possible.

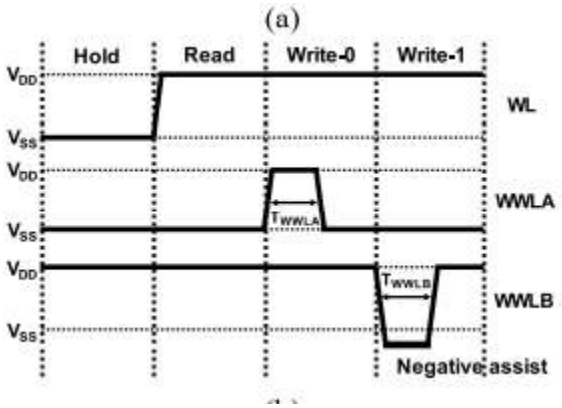

Fig 5. Simulation of One sided schemit trigger schematic simulation

Content Production, Level B The specifics of The type of data that is being stored affects how the write process is performed. The results of a write-zero operation are seen in figure 6.. During a process known as a write 0,BL is set to 0, the column-based WWLB is maintained at 1, and WL is enabled by the write driver. By setting the WWLA column to 1, By gating power to Node Q with the value 1, the connection to the VDD power source that was previously established through PUL2 is severed. The power-gated Q node needs to be set to zero for the activated PG to be able to invert the ST. After When the WWLA column is set to "0," all data is deleted from storage. for node QB will be flipped around.50% of all cells in a given column are considered. Pulse width of WWLA (TWWLA) will be discussed in further depth in the following section. following section.

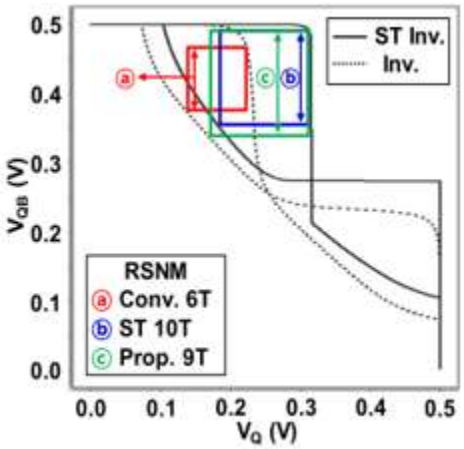

Fig 6 :Power Analysis of One sided schemit trigger schematic simulation

The one-sided schemit trigger simulation results are shown in the above figure along with an average power analysis of one-sided schemit trigger 9T SRAM; the proposed model's average power consumption is 358.78 microwatts.

Instead of employing a series of PGs Similar to a single PG is used in the Chang This is true for the current generation of SRAM cells (10T, MH 9T, and ST 9T) and the future generation of ST 9T SRAM cells. Because PUL2 is turned off during the write-0 process, the route will lose power. Because of this, we can infer that the ST 9T SRAM cell has adequate write-0 capability. Figure 5 depicts a real-world instance of a write-1 operation. When write-1, BL is set to 1, allowing for WL writing but not altering the column-based WWLA. When the value in the WWLB column is "0," the PDL1 power gate is used to cut off the VSS power supply at node Q, and the value "0" is stored. This allows the ST inverter to be used in normal applications. The ST inverter can be inverted by activating the PG, which will then allow the power-gated Q node to be set to the position "1." Following the inversion of the data contained within node QB, the WWLB column orientation will be brought back to "1." In the process of determining how long a WWLB pulse will last, the column half-selected cell will be taken into account (TWWLB). The procedure for The write-1 operation begins when the VSS power supply is disconnected, just as it does during the write-0 process. Despite this, we can't do more because nMOS PG has terrible write-1 drivability. assures that the write-1 address can be used for outgoing data. The proposed ST 9T SRAM cell makes use of a novel method called negative VWWLB help to boost write-1 performance. When the WWLB is set to 0 and the NF is activated, there is a dramatic drop in voltage at the Vx node. The ST inverter's trip voltage will drop in tandem with a decline in Vx as PDR1 strength increases. A write-1 is significantly easier to do. During the course of the test, the trip voltage will fluctuate as shown in Figure 7. Setting WWLB to "0" in the write-1 operation decreases the ST inverter's trip voltage by 21.9% due to the elimination of the feedback mechanism and the convergence of its function with that of the inverter. This is because the ST inverter's purpose is more closely aligned with that of the inverter. When the WWLB voltage drops below -0.2 volts, it trips. This is a 52.4% reduction from the original value. If the trip voltage can be reduced, the negative VWWLB aid strategy has the potential to greatly increase the write-1 capacity.

5.RESULTS

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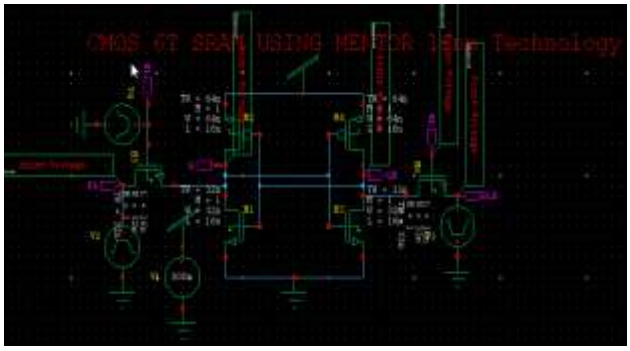

FIG 7 :SRAM 6T Schematic

An illustration of a read-disturbance cell that has a bumped storage node may be found in Fig. 7. The read stability of both the ST 10T and the soon-to-be-released The ST inverter enhances the performance of ST 9T SRAM cells. The occurrence can be attributed to these several causes. Read disturbances cause NFL to temporarily be enabled when the node Q of the "0"-storing ST 10T SRAM cell is disturbed. VXL that occurs as a result of NFL causes the strength of PDL1 to decrease. This suggests that the read disruption will become much more noticeable in the future. However, by utilising a crosscoupled architecture, the ST 9T SRAM cell that is currently in development can get around this problem. This suggests that the read disruption will become much more noticeable in the future. The ST 9T SRAM cell that has been suggested, on the other hand, gets around this problem by employing a crosscoupled topology that combines ST and normal inverters. This is feasible since the single BL contains a storage node with the designation Q. structure only ever encounters read disturbances when it is set to "0."

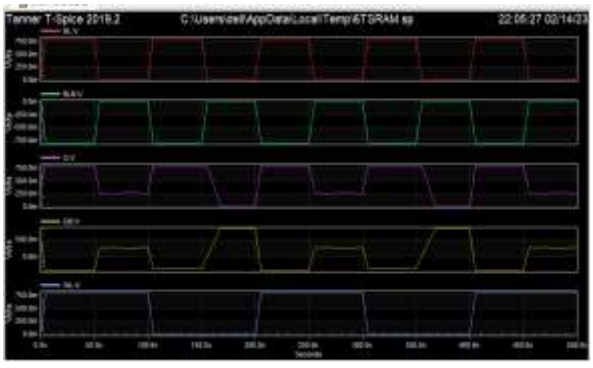

FIG 8: SRAM 6T Schematic simulation

PROPOSED 9T SRAM-SCHMITT TRIGGER

Figure 9 is the proposed ST 9T SRAM cell's BL layout design and timing diagram. The proposed ST 9T SRAM cell has a regular stacked-transistor inverter (PUL1, PUL2, PDL1, PDL2), a ST inverter (PUR, PDR1, PDR2, NF), and a nMOS PG. WL signals are row-based. Column-based signals include WWLA and WWLB.By way of illustration, WL is able to talk to PG's gates, while PUL2's gates can talk to

WWLA. In addition to the PDL1 gate, the WWLB is also linked to but also to the NF source. Option A: Carry Out Operations During the reading process, PUL2 and PDL1 will be activated only if both WWLA and WWLB return the value "0." The shared inverter provides electricity to the storage node designated by the letter Q. Both the WL and PG are actively being activated at the same time. After then, the BL is either allowed to be released or it is not allowed to be released based on the information at node Q. Interference from BL is a typical factor that can contribute to failed reads. When an unexpected read disruption occurs bumps The data that has been stored could be corrupted if the storage node's voltage is greater than the threshold at which the inverter activates. The proposed ST 9T SRAM cell has a cross-coupled architecture that mixes conventional and ST inverters to prevent this kind of read failure from occurring. DC features of the ST inverter are depicted in Figure 9, and its schematic can be found in Figure 10.

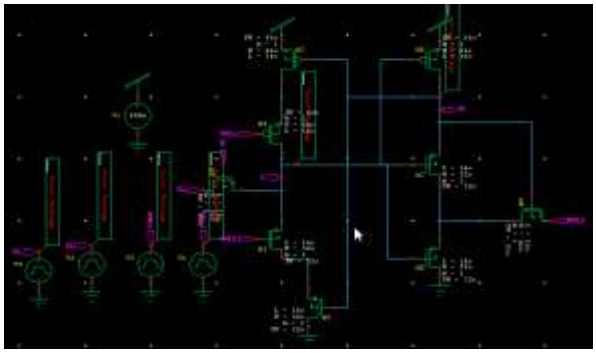

Fig 9 One sided schemit trigger schematic simulation

compared to the voltage that is generated by a regular inverter. The feedback transistor NF increases VX while simultaneously lowering the intensity of PD1 signal. The ST inverter is able to withstand a one-unit spike to the storage node without causing as much read disruption as a normal inverter would due to the fact that this is the case. Read-disturbance bumping storage node Figure 9 depicts cells in each stage. The ST inverter improves read stability of the ST 10T and soon-to-be-released ST 9T SRAM cells. The suggested ST 9T SRAM cell also provides superior read stability than cross-coupled ST inverter ST 10T SRAM cells.The occurrence can be attributed to these several causes. When node Q detects a read disturbance, it writes the value "0" into the ST 10T SRAM cell. bumps occur. At this point, NFL is turned on very slightly, and the subsequent increase in VXL generated by NFL leads PDL1 to weaken. This suggests that the read disruption will become much more noticeable in the future. The ST 9T SRAM cell that has been suggested, on the other hand, gets around this problem by an architecture that combines ST and standard inverters and uses a crosscoupled configuration. This is possible because the read disturbance in the one-of-a-kind BL structure only takes place when storage node Q is equal to 0. This hypothesis was verified through an examination of the butterfly curves of read-disturbance cells. Figure 5 depicts the read static noise margins (RSNMs) of various types of batteries, including SRAM batteries, ST 10T batteries, and conventional 6T batteries. In order to calculate the RSNM, you need

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only measure the length of town square. Given the ST 9T SRAM cell's asymmetrical layout, the RSNM increases when Q stores a "1" rather than a "0." Not even the fact that Q stores the identical value could change this. The proposed ST 9T SRAM cell accounts for the worst-case RSNM, making it comparable to existing SRAM cells. The ST inverter's higher trip voltage increases the ST 10T SRAM cell's RSNM. Reason: ST inverter trip voltage is greater. The ST 10T SRAM cell has the highest RSNM, although the ST 9T has less side effects.

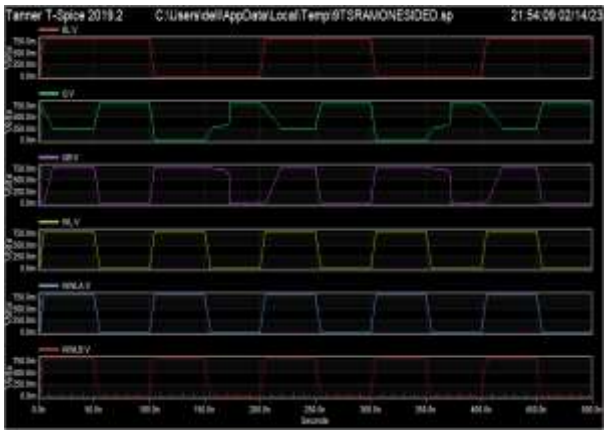

Fig 10 Simulation of One sided schemit trigger schematic simulation

Methods for Scripting at the Level B The write procedure is different each time since it is determined by the data that is being written. The results of a write-0 operation are shown in figure 6, which may be found here (a). Whenever If you are performing a write-zero operation, the write driver will set BL to "0," and WWLB for the appropriate column will continue to be set to "1;" nevertheless, WL will be enabled. In the event that the value "1" If kept in Node Q, the WWLA column is set to 1 (i.e., power is switched off), supply to the path from VDD by turning off PUL2. When the PG is activated, the power-gated Q node is set to zero, which toggles the ST inverter. Following the reversal of the node QB's stored data, the WWLA column is reset to "0." In particular, Pulse width of WWLA (TWWLA) is calculated by factoring in the column half-selected cell. something that will be detailed in further detail in the section that comes after this one. the events that followed section.

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Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 2.979741e-07 watts
Max power 4.108794e-06 at time 1.72596e-07
Min power 6.784704e-08 at time 6.25e-10
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Fig 11.Power Analysis of One sided schemit trigger schematic simulation

The one-sided schemit trigger simulation results are shown in the above figure along with an average power analysis of one-sided schemit trigger 9T SRAM; the proposed model's average power consumption is 358.78 microwatts.

In place of a string of PGs, we will be employing Similar to Chang's 10T and MH's 9T SRAM cells, the proposed ST 9T SRAM cell will use a single PG. Because PUL2 is turned off during the write-0 process, the route will lose power. This means the specified ST 9T SRAM cell has enough write-0 space. Figure 5 depicts the write-1 operation. The write driver will enable the WL by setting BL to 1 during the write-1 operation. Nonetheless, WWLA calculated on a column basis will remain unchanged at 0. The value of the WWLB column being "0" causes PDL1 to be disabled, and the node Q that stores "0" is also disabled. As an added bonus, when a ST's feedback mechanism After the trip voltage is set to mimic that of a standard inverter, the inverter can function as if it were not connected to the battery. When the feedback system is disabled, an appropriate adjustment is made. When the power gate is on, the process ST inverter is flipped by setting the power-gated Q node to 1. As the information in node QB has been reversed, the WWLB column now has the value 1. The pulse width is calculated by factoring in the number of cells in the column that were half-selected. with respect to WWLB (TWWLB) (TWWLB). The write-1 process is launched in the same way that the write-0 operation is, by breaking the VSS power connection. Due to nMOS PG's poor write-1 drivability, it is unable to provide an adequate guarantee of the write-1 capability. Because of this, provision is impossible. Using the negative VWWLB boosts the write-1 capacity of the proposed ST 9T SRAM cellHelping out is the way to go. Threatening extinction: WWLB is on the verge of When the NF is engaged, the voltage at the Vx node immediately lowers. With an increase in PDR1 intensity and a decrease in Vx, the ST inverter's trip voltage is dramatically lowered. This simplifies the write-1 process. Figure 7 shows the dramatic range of voltage fluctuations encountered throughout the trip. When WWLB is set to "0" in a write-1 operation, the ST inverter's feedback mechanism is deactivated, reducing the ST inverter's trip voltage by 21.9%. This happens because the ST inverter's trip voltage eventually reaches the same level as the inverter's. WWLB's trip voltage is reduced by 52.4% when subjected to a negative voltage of -0.2 V. A significant improvement in write-1 capacity may be possible using the negative VWWLB support method. The reduction in the trip voltage makes this possible.

CONCLUSION

Low energy consumption has become important for bio implants and mobile devices because they need to operate with limited energy. Operating the SRAM in the near-Vth region is crucial for reducing energy usage. A one-sided ST 9T SRAM cell with high read stability, write capability, and hold stability yields around Vth is proposed in this work. The read stability yield of the proposed ST 9T SRAM cell was enhanced by using a cross-coupled combination of standard and ST inverters. Furthermore, the proposed ST 9T SRAM cell assured a 5 target write ability yield by applying selective power gating and

a revolutionary negative VWWLB assist strategy that regulated the trip voltage of the ST inverter. The planned ST 9T SRAM cell is smaller in size than Chang's 10T, ST 10T, and MH's 9T SRAM cells. The proposed ST 9T SRAM consumes much less energy than Chang's 10T, the ST 10T, and MH's 9T SRAMs at each Vmin_energy, although it has a larger read delay owing to the single BL structure. As a result, the proposed ST 9T SRAM cell has the best near-Vth EDP

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