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A NOVEL APPROACH TO DESIGN A HIGH PERFORMANCE 10T SRAM WITH HIGH RECOVERABILITY OF MULTI-NODE SOFT ERROR

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ABSTRACT

Aerospace SRAM cells have a lower critical charge of sensitive nodes, making them more prone to soft errors. SRAM cells in aeronautical applications cause this. Radiation hitting a sensitive node in a conventional 6T SRAM cell causes a single-event upset. Many factors can cause this. The cell's data is now in the improper order (SEU). This research proposes the Soft-Error-Aware Read-Stability-Enhanced Low-Power 12T (SARP12T) SRAM cell to prevent SEUs. The performance Ts of the SARP12 are compared to those of the publicly available soft-error-aware SRAM cells QUCCE12T, QUATRO12T, RHD12T, RHPD12T, and RSP14T. SARP12T-sensitive nodes will receive their data even if radiation inverts node values. SARP12T may recover from the single-event, multi-node disturbances caused by storage node pairing (SEMNUs). The proposed cell has industry-leading read stability. The bitline directly accesses the noise-resistant storage node that stores "0" during the read operation. The bitline can reach the node even when reading. The SARP12T uses the least power in hold mode. The SARP12T also beats most comparable cells in write performance and has a far lower write latency. The SARP12T features newer, more advanced technologies. The recommended cell's full benefits can be realised by slightly increasing the read delay and write energy. Notwithstanding the delay.

Keywords: — Single-event upsets (SEU) and single-event multinode upsets (SEMNUs), critical charge, radiation hardness, read stability, hold power, and write ability are some of the characteristics that can be measured.

1.INTRODUCTION

By providing satellite communications, military surveillance, navigation, and tracking systems, aviation has improved quality of life.Aircraft microprocessors perform many tasks. Control, directing, engine management, and inertial navigation are examples. Each CPU has many processing cores that work together to boost performance.Cache data matches processing cores [2]. SRAM cells as cache memory are essential for CPU power, space, and latency optimization.Particles from space with extremely high

energy may affect memory circuit efficiency. [3] . The integrated circuit can eject a charged particle. The strike-produced minority carriers interpret the forward electric field when a reverse bias is applied between the substrate/n-well and the diffusion zone.

Minority carriers go towards drain diffusion zones because of this. Depending on their type, minority carriers can clump together to generate a positive or negative voltage spike. Before or after minority carriers arrive. If the spike's amplitude and length are large enough, single-event upset (SEU) or soft-error will occur, overwriting previously stored information [4, 5]. This is a soft mistake. Soft error (SEU) Technology is shrinking the minimum distance between integrated circuit components [6,] so a single ion assault could damage multiple nodes (SEMNU).Triple modular redundancy reduces SEUs' memory damage (TMR). This method employs a majority vote to select which of three replicated memory cells has the right value and outputs it [7, 8]. Voting on the other two copies will continue normally even if one copy is flipped. It requires a lot of area and energy, hence most designs fail [8, 9].SEUs can also be mitigated via error-correcting codes (ECCs). Due to redundancy and encoding and decoding circuit devices, ECCs require a lot of power, space, and delay [10]. ECCs need encoding and decoding devices [10].Soft-error-aware SRAMs are better than ECCs because they require less power and delay. SRAM cells should be resilient enough to recover from multi-node disruptions.

2.LITERATURE SURVEY

Soft Error Hardened Memory Design for Nano-scale Complementary Metal Oxide Semiconductor Technology The current major cause of reliability loss in nanoscale memory is radiation-induced soft errors, also known as single event upsets (SEUs). As a result of this research, a novel complementary metal oxide semiconductor (CMOS) memory cell is proposed, which uses minor error hardening in 65 nm technology. The appropriate topology for the design, as well as the SEU physics technique, provide its basis. The design process includes a thorough examination of the pros and disadvantages of different types of hardened memory cells in terms of read/write access times, power consumption, and layout area.

The suggested cell has a 100% fault tolerance, making it ideal for use in memory applications even when exposed to high levels of radiation. The results of process, voltage, and temperature changes are also analysed using Monte Carlo simulations (PVT).Our modelling work indicates that the proposed cell can withstand several node upsets, even in the presence of PVT fluctuations. Single-event upsets (SEUs) are thought to reduce the reliability and availability of Nano-scale memory devices [1, 2, 3]. SEUs are induced by radiation particles (such as protons, neutrons, and electrons) created by packaging materials and cosmic rays.Miniaturization of CMOS technology has decreased supply voltage and decreased node capacitance [4]-[7], making memory cells more vulnerable to radiation particles. A SEU can alter the behaviour of memory cells, leading to an unexpected failure of the electrical system [4].

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3.EXISTING METHOD

Figure 1 provides an illustration of the layout and configuration of the SARP12T. Four distinct elements make up SARP12T: two wordlines (WL and WWL), two internal nodes (S1 and S0), and two storage nodes (Q and QB). A pair of WL-controlled access transistors, designated as N7 and N8, are responsible for making the connection between the storage nodes Q and QB and the BL and BLB lines. The WWL-controlled access transistors N9 and N10 provide the connection between the internal nodes S1 and S0 and the bitlines BL and BLB. As a point of departure, we will make use of SARP12T in addition to any additional comparison cells that already have the value "1" (Q will be set to "1," while QB will remain at "0"). As a consequence of this, the values of S1 and S0 are, respectively, "1" and "0." This information is taken into consideration when conducting SARP12 base T operations and SEU recovery investigations.To disable the WL and WWL pairs, the hold mode forces their access transistors to GND. Hold mode keeps bitlines at VDD potential to cut down on read delay.

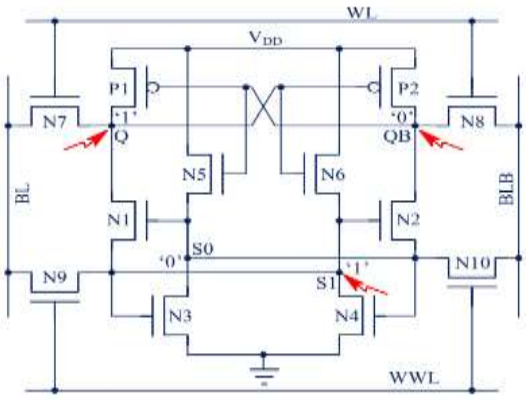

Fig 1. SRAM with multi-node soft error

Because of this, the hold state of the cell results in only the transistors P1, N2, N3, and N6 being active. Because of this, SARP12T continues to make use of the information that it first saved (Fig. 3). The write operation, which is step two, makes use of both the WL wordlines and the WWL wordlines. As a consequence of this, the pairs of access transistors N7/N8 and N9/N10 are activated. The saved information can be modified by connecting BL to GND and clamping BLB at VDD (i.e., write "0" at Q). Nodes N7 and N9 are responsible for bringing down nodes Q and S1 when BL is connected to GND. To counteract the effects of node S1's deactivation of nodes N2 and N3, node Q activates node P2 and deactivates node N6. At nodes N8 and N10, BLB receives both QB and S0 concurrently. The states of P1 and N5 are thus controlled by Node QB. When node S0 is activated, nodes N1 and N4 are as well. With P1 and P2 in cross-coupling, the potential gap between Q and QB is widened. The potential difference between S1 and S0 is so increased, in a manner analogous to the cross-coupling between N3 and N4. That means the write went through without a hitch.

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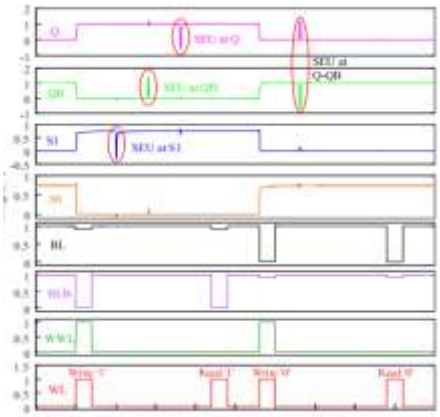

Fig 2 simulation results of SRAM with multi-node soft error

During a read operation, WL is connected to VDD unless WWL is present. Hence, N7 and N8 become active while N9 and N10 remain inactive as access transistors. While reading, the bit lines are initially charged to VDD. Therefore, BLB can easily disperse across the N8, N2, and N3 pathways. Since neither N1 nor N4 are currently operational, BL will continue to reside at VDD (Fig. 3). As soon as there is a 50 mV gap between BL and BLB, the read process is complete, and the data can be picked up by a detecting amplifier (not shown).

4.PROPOSED METHOD :

we-Quatro: Radiation-hardened SRAM Cell

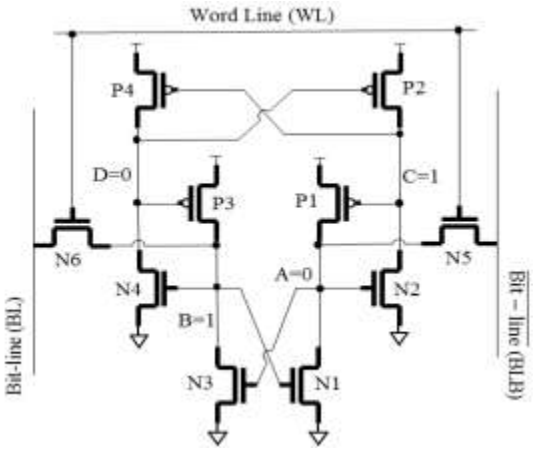

Fig 3 we-Quatro: Radiation-hardened SRAM Cell

This issue is going to be addressed by the brand-new radiation-resistant SRAM cell called the We-Quatro. For the remainder of this text, the word "we" shall stand in for the phrase "writability increased" because we wish to keep things as brief as possible. The Quatro SRAM cell has a total of 12 transistors,

but it has an additional pair of access transistors for improved writability. This brings the total number of transistors to 14. Because it takes advantage of the space-reduction capabilities of the SRAM cell architecture, the we-Quatro architecture that we propose uses the same volume of cells as the Quatro architecture. We use Monte Carlo (MC) simulations to determine whether or not our proposed SRAM cell can be written to. In spite of the fact that parametric process instabilities exist, the results demonstrate that We-Quatro offers sufficient writability for 28nm FD-SOI technology. When designing SRAM, it is essential to take into consideration the read static noise margin, the read accessing stability, and the writability of the memory. As a result, we compared the features of the we-features Quatro to those of the original Quatro. It is essential to keep in mind that the objective of this work is to develop a method that can be scaled up to produce radiation-resistant SRAM cells. As a result, we simulate the necessary conditions in order to evaluate the robustness of these cells against soft mistakes. The results of these quantitative comparisons demonstrate that our proposed SRAM cell functions quite well. After that, we conduct an analysis of our proposed SRAM cell and investigate the dependability of our we-Quatro with regard to prospective scaling methods.

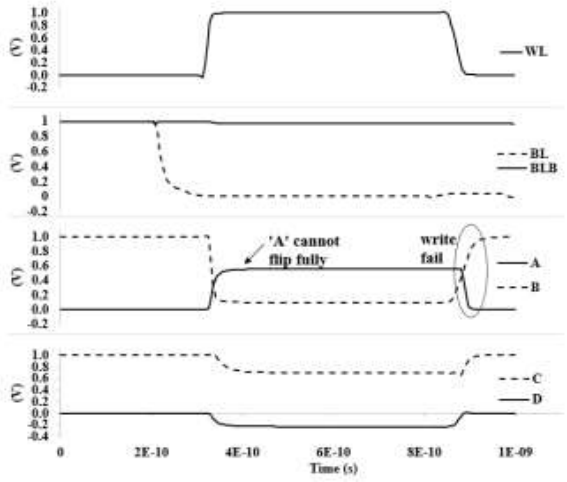

Fig 4 simulation of we-Quatro: Radiation-hardened SRAM Cell

A simplified representation of a quadro cell, which consists of four memory hubs that are coupled to one another, can be seen in Figure 3. Example 2 (A, B, C, and D). Soft errors are prevented by design [9]. A storage node communicates with the gates of both PMOS and NMOS transistors in a typical six-transistor static random access memory (SRAM) device. Changes to the cellular data occur whenever a single event transition (SET) either increases or decreases the pull-up strength of PMOS. A storage node's only responsibility in an interlocked Quatro architecture is to serve as the gate input for two complementary PMOS or NMOS transistors. This is the storage node's sole function. A SET in this setup can change whether NMOS or PMOS transistors behave as pull-up or pull-down. Nonetheless, complementary transistors' functionality for soft-error avoidance is unaffected. Note how the voltage at node 'B' in Figure 2 decreases over time as a result of exposure to radiation. Possible reduction in N1

and N4's pulling power due to this SET. Voltages "A" and "D" seldom ever shift because P1 and P4 are immune to this background interference. So, after a fixed amount of time, "Bvoltage "'s resets to the supply level. The data included in the first cell is therefore inaccessible to this SET.

5.SIMULATION RESULTS

EXISTING METHOD

The layout of the SARP12T, which can be seen in Figure 5., is comparable. Four different nodes make up SARP12T: two for storage (Q and QB), two for internal processing (S1 and S0), and two for wordlines (WL and WWL). A pair of WL-controlled access transistors, designated as N7 and N8, are responsible for making the connection between the storage nodes Q and QB and the BL and BLB lines. Through the access transistors N9 and N10, BL and BLB are connected to the internal nodes S1 and S0. WWL is the one in charge of controlling these transistors. Examine the SARP12T cell as well as any additional cells that have a "1" (Q equals "1," whereas QB equals "0"). Both S1 and S0 have values of one (1) respectively. With this in mind, we will now analyse the functioning of the SARP12fundamental T as well as its SEU recovery. In this section, we will discuss SARP12T.Hold mode involves disabling both sets of access transistors by connecting WL and WWL to GND. This is done so that the hold mode can be used. While in hold mode, bitlines are maintained at VDD in order to increase the speed of readings.

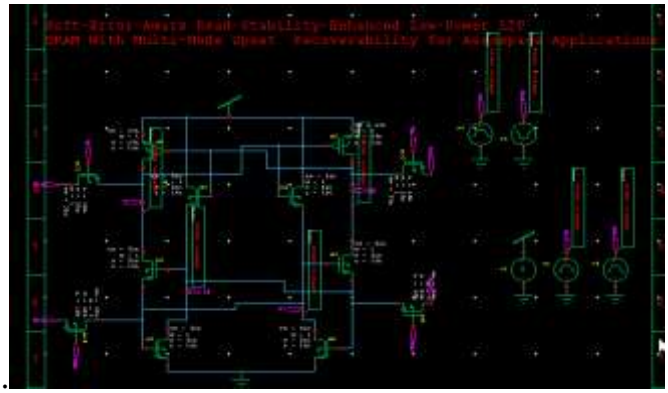

Fig 5 SRAM with multi-node soft error

While the cell is in the hold state that it is currently in, only the transistors P1, N2, N3, and N6 are active. Because of this, SARP12T does not make any changes to its data (Fig. 5). During the write operation, both the WL and WWL wordlines are active and functioning normally. As a consequence of this, the pairs of access transistors N7/N8 and N9/N10 are activated. We are able to make changes to the information that has been saved if we connect BL to GND and clamp BLB to VDD (i.e. write "0" at Q). Because that BL is linked to GND, it is bringing nodes Q and S1 down by way of nodes N7 and N9, respectively. Node Q turns on the power to node P2 and turns off the power to node N6, and node S1 turns off nodes 2 and 3. Both BLB and QB can be accessed through N8 and N10, respectively. As a

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result, the QB node activates Node 5 and deactivates Node 1. In a manner analogous to this, S0 sets off N1 and N4. Due to the fact that P1 and P2 are cross-coupling, the potential difference between Q and QB has become greater. Thus, in a manner analogous to that of N3-N4 cross-coupling, raises the potential between S1 and S0. So, the process of writing was successful.

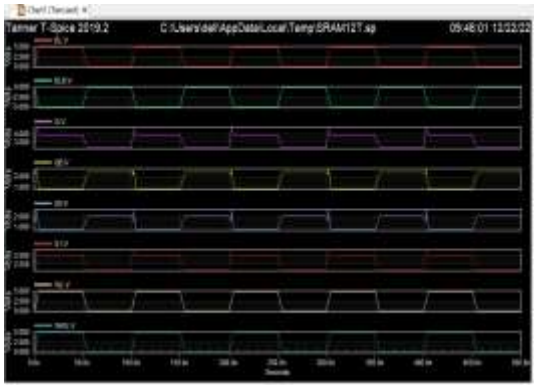

Fig 6.simulation results of SRAM with multi-node soft error

While a read operation is being performed, if WWL is not active, then WL will be wired to VDD. Access transistors N7 and N8 are activated due to the fact that N9 and N10 are not being utilised. Whenever reading is being done, the bit lines will first be charged to VDD. As a direct consequence of this, BLB is released by the neurotransmitters N8, 2, and 3. Despite this, BL is still set to VDD even if N1 and N4 have been switched off (Fig. 6). The read operation might be stopped by a detecting amplifier if the difference in voltage between BL and BLB is more than 50 millivolts (not shown).

PROPOSED METHOD :

we-Quatro: Radiation-hardened SRAM Cell

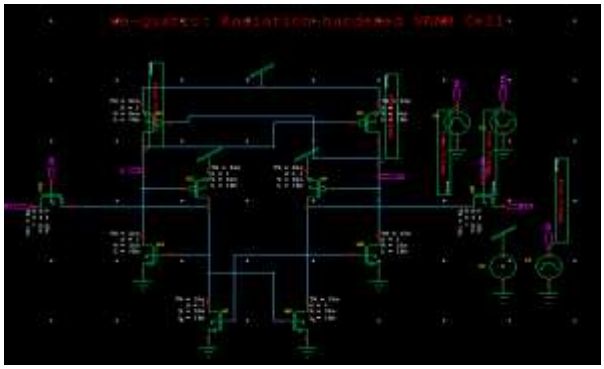

Fig 7: we-Quatro: Radiation-hardened SRAM Cell

We-Quatro, a novel radiation-resistant SRAM cell, is being offered as a possible answer to this problem. We stand for "improved writeability" here. The proposed SRAM cell for Quatro has a total of 12

transistors, with 14 added access transistors for improved write performance. But, we-Quatro uses exactly the same amount of cell space that Quatro does since we take advantage of the benefits of SRAM cell architecture. Monte Carlo (MC) simulations are used to ascertain whether or not our proposed SRAM cell is writable. The outcomes show that we-Quatro offers sufficient writability for 28nm FD-SOI technology regardless of the process parameter fluctuations. Read static noise margin, read accessing stability, and writeability are all important factors to think about when designing SRAM. For this reason, we evaluate the improvements made by the new Quatro in relation to its predecessor. It's worth noting that this study aims to find ways to mass produce SRAM cells that can withstand radiation. We do the necessary simulations to evaluate the cells' resistance to soft errors. The results of these comparisons provided strong evidence for the efficiency of our suggested SRAM cell. We then examine the reliability of our we-Quattro across a wide range of scaling conditions after analysing our suggested SRAM cell.

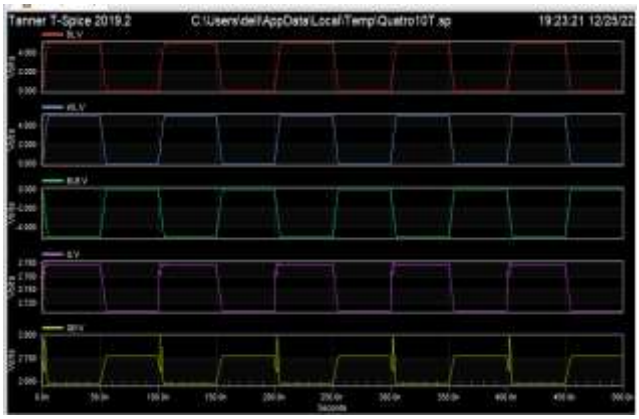

Fig 8 simulation of we-Quatro: Radiation-hardened SRAM Cell

A schematic representation of a quadro cell displaying four connected storage nodes may be found in Figure 8. (Figure 2, letters A, B, C, and D). Because of the architecture, there is far less room for making small errors. Within a typical 6T SRAM, the gates of both PMOS and NMOS transistors have the ability to retrieve data from a storage node. When a SET either enhances or weakens the pull-down of NMOS or the pull-up of PMOS, the information that is stored in the cell is switched around. On the other hand, with an interlocked Quatro arrangement, the storage node serves as gate input for only two of the PMOS or NMOS transistors. In this design, a SET can either lessen the amount of pull-up or pull-down that PMOS or NMOS transistors experience, or it can make the effect stronger. In spite of this, the efficiency of complementary transistors in the prevention of soft errors is unaffected by the situation. Imagine that, as a result of being exposed to a radiation particle, the potential of the node labelled "B" in Figure 2 begins to slowly decrease. This SET has the potential to reduce the amount of pull-down force exerted by neurons N1 and N4. P1 and P4 are not affected by the noise, which means that the "A" and "D" voltages hardly ever change. As a result, "Bvoltagewill "'s restore to supply level once a predetermined

length of time has passed. As a direct consequence of this, this SET is unable to acquire the information pertaining to the primary cell.

```
   Opening simulation database "C:\Users\dell\AppD

Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 1.559360e-03 watts
Max power 6.063728e-02 at time 2.61813e-09
Min power 2.217735e-08 at time 3.5486e-07


Measure information will be written to file "C:\Us

Measurement result summary
   tdealy          =  52.2219n
```

Table :1. Comparison between 12T with 10T

S.NO	Method	No:Transisitors	Power	Delay
1	90nm	12	4.463	100.01n
2	16nm	10	1.53 mw	52.2219n

CONCLUSION

In this study, we propose a novel we-Quattro SRAM cell that can withstand high levels of radiation. One of the most promising radiation-hardened SRAM cells, Quatro, suffers from poor writability when subjected to the parametric process modifications used by scaled technologies. As simple as adding two more access transistors, this problem can be easily fixed. We take advantage of Quatro's thin-cell design because of its merits. The we-Quatro cell area is identical to that of the Quatro cell, despite the fact that more transistors have been added. Extensive simulations show that for 16nm CMOS technology, we-Quatro performs better than Quatro. We additionally test the we-Quatro, Quatro, and 6T SRAM for their resilience against soft errors using appropriate simulations. According to the study, We-Quatro is more robust than 6T SRAM and has soft-error immunity on par with Quatro. We think precautions need to be taken with regard to machinery that could be exposed to radiation.

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