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FPGA IMPLEMENTATION OF 32 BIT VEDIC MULTIPLIER USING VERILOG HDL

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***Abstract*—To meet the demands, complicated and difficult activities must be handled in processors, which results in an increase in processing cores. This increases the stress on the processor, which can be reduced by assigning coprocessors to particular types of tasks, such as signal processing. However, the ALU's response time is based on the multiplier's speed. Given that multipliers are crucial parts of the CPU that carry out operations. Vedic mathematics is used to execute quick multiplication operations, and it is based on 16 sutras, each of which has unique properties. This method typically lowers the processors' space, power, and delay. The Vedic multiplier algorithms known as Urdhva Tiriyagbhyam and Nikhilam, which are based on two distinct sutras, have therefore supplanted the current Wallace tree multiplier technique. Verilog HDL was used to design and specify these multipliers, and Xilinx ISE project Navigator was used to synthesize and simulate them.**

Keywords— Vedic multiplier, ALU ,Verilog HDL.

I. INTRODUCTION

Multiplication is a very essential arithmetic operation and extensively used in microprocessors, microcontrollers and digital signal processors which is a time consuming operation because it takes more time and clock cycles as compared to other arithmetic operations. It is found from the various proposed architectures in literature that Vedic multipliers are faster than non-Vedic multiplier architectures. Different architectures have been proposed in literature to improve the efficiency of multiplication using Vedic mathematics. These architectures are based on conventional Vedic, Vedic using RCA, Vedic using addition tree structure and Vedic using CSA The Vedic multiplier algorithms known as Urdhva Tiriyagbhyam and Nikhilam, which are based on two distinct sutras, have therefore supplanted the current Wallace tree multiplier technique. Verilog HDL was used to design and specify these multipliers, and Xilinx ISE project Navigator was used to synthesise and simulate them. According to evolving technology, any proposed system must be effective in terms of power, speed, and size. 16 Vedic sutras served as the foundation for early Vedic mathematics. Mathematical processes are quick when performed utilising Vedic methods, and processing speed can be increased. There are numerous effective binary multipliers already in existence. The binary Vedic multiplication technique is modified in the current work. The current paper follows: Section II describes problem definition. Section III explains the rules for multiplication process and also explains the existing and proposed methods for the 32 bit Vedic multiplier. Section IV contains the methodology. In section IV, a better modified 32-bit binary Vedic multiplier is created. The paper's results are displayed in Section V, along with a comparison to earlier approaches. The conclusion of this essay is provided in Section VI.

II. PROBLEM DEFINITION

The Vedic multiplier that has been proposed is based on the sutras for Vedic multipliers. In the decimal number system, these sutras have historically been used for multiplication of two numbers. To make the suggested algorithm compatible with the digital hardware, apply the same principles to the binary number system.

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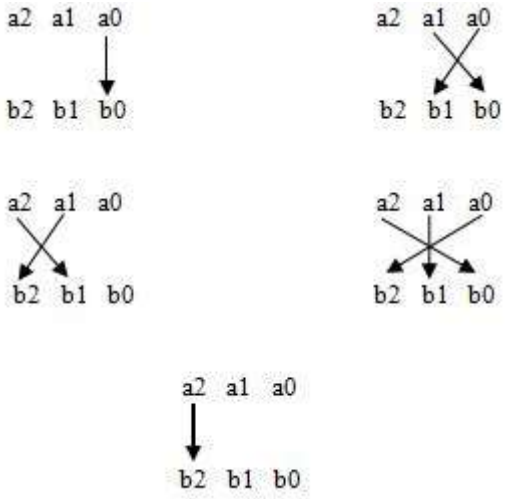
III. **RULES & BLOCK DIAGRAM EXPLANATION**

The 16 Vedic sutras that form the foundation of the Vedic multiplication system give natural solutions to a wide variety of mathematical issues. The Urdhva-Triyakbhyam sutra, one of these 16 Vedic sutras, has a universal multiplication formula. Literally, it means crosswise and vertically.



BLOCK DIAGRAM EXPLANATION:

EXISTING METHOD:

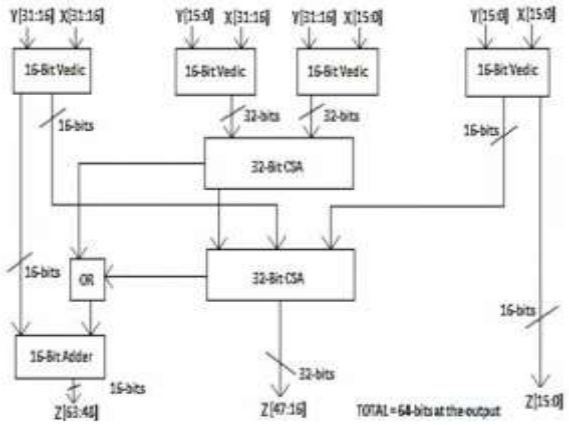


Fig.1.Existing 32-Bit Vedic Multiplier

The multipliers are the most crucial component of any digital signal processors since they enable several crucial operations including convolutions and fast Fourier transformations (FFT). Long multiplication has a version known as the Wallace Tree. Multiplying each digit of one element by each digit of the other is the first step. Each of these partial products is equivalent in weight to the sum of its constituent parts. The weighted sum of each of these partial products is used to determine the final product. An increase in multiplication speed can significantly boost system performance because multiplication takes a significant amount of time on a CPU. The time it takes for signals to go through the gates coming from the multiplication

array is the delay connected to the array multiplier. For high-speed multiplication and exponential calculations, huge booth arrays are needed, which in turn call for big partial sum and partial carry registers.Thus the system becomes complex.

PROPOSED METHOD:

One carry save adder is presented as a 32-bit Vedic multiplier. In order to reduce the number of hardware blocks in the circuit, the input of the multiplier is set up as two 16-bit values, and it is applied sequentially using the Urdhva Tiryagbhyam sutra. The partial product is then added using a single carry save adder.

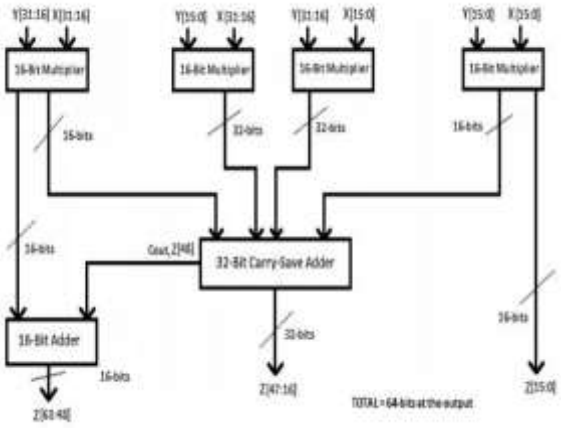


Fig.2.Proposed 32-Bit Vedic Multiplier

IV METHODOLOGY

Using RCA, a 2-bit Vedic multiplier is first designed, and in the same way, its size is increased up to 32 bits, or 4, 8, 16, and 32 bits, using CSA. After that, a modified 2-bit Vedic multiplier is implemented, and in the same way, its size is increased up to 32 bits, or 4, 8, 16, and 32 bits, using RCA. Utilizing the XILINX ISE DESIGN SUITE, the final synthesis is carried out. The use of two half adders is suggested for a 2-bit Vedic multiplier. The use of one carry save adder is suggested for a 4-bit Vedic multiplier. Utilizing the Urdhva Triyagbhyam sutra, the multiplier's input is split into two 2-bit values for stepwise application, and the partial product is added using a single carry save adder to reduce the amount of hardware components in the circuit. Similar to how we utilised two 4-bit numbers for 8-bit, two 8-bit numbers for 16-bit, and two 16-bit numbers for 32-bit, we did the same for 8-bit.Literally translated as "vertically and crosswise," the Vedic Multiplier. By multiplying two operands using the VEDIC multiplier both vertically and crosswise, and then adding the results, two operands are multiplied. A good multiplier should have three main characteristics: high speed, low power consumption, and small size. Vedic multipliers are the quickest and take up the least space. They have as their foundation the Vedic mathematics sutra "Urdhava-Triyakbhyam". The use of multipliers in VLSI is used in the design of many kinds of hardware and software multipliers. this algorithm is used to reduce the number of partial product rows by about half , so, the speed of multiplication increases significantly and the chip area is reduced. Vedic Multiplier utilizes a total of 16 sutras, primarily for logical processes. They have all been put forth using the Urdhva-Triyagbhyam sutra, making them the most effective in terms of speed.

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V RESULTS

The suggested work leverages XILINX ISE project navigator for synthesis and Verilog HDL simulation. The simulation can handle operations up to 32 bits in size

Table 1: Requirements for modified 32-bit Vedic Multiplier

S .No.	Bit Size	Basic Design Units
1.	2x2	Four AND gates and Two Has.
2.	4x4	Four 2x2 bit multipliers, CSA for 4-bit addition, OR gate, 2bit adder.
3.	8x8	Four 4x4 bit multipliers, CSA for 8-bit addition, OR gate, 4bit adder.
4.	16x16	Four 8x8 bit multipliers, CSA for 16-bit addition, OR gate, 8-bit adder.
5.	32x32	Four 16x16 bit multipliers, CSA for 32-bit addition, OR gate, 16-bit adder.

The waveform of simulation for modified 32-bit Vedic multiplier shown in Fig 3.
Simulation was performed using Xilinx ISE Project navigator. The RTL simulation results for a 32x32 bits Vedic Multiplier are shown in figure 3, in which the input 1=E19FAB and input 2 =59ED2A then we got the output=4F418848810E.

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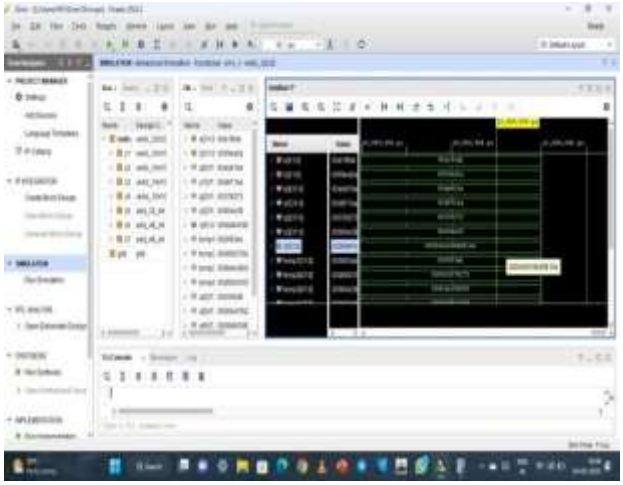

Fig.3. Simulation Waveform for Modified 32-Bit Vedic Multiplier.

The proposed technology is more effective than current techniques in terms of time delay. With the aid of the suggested technique, elongation for a larger bit size can be accomplished. Additionally, the CSA Carry Save Adder design utilised in the proposed modified Vedic multiplier allows for the usage of adders with various architectural styles. Modified architecture is one of the methods used to boost and speed up multiplication.
The synthesis report for the 8 bit Vedic Multiplier is shown below. Here we used 7 cells, 32 I/O ports and 81 Nets to design the circuit. similarly we can get the design for 32 bit also.

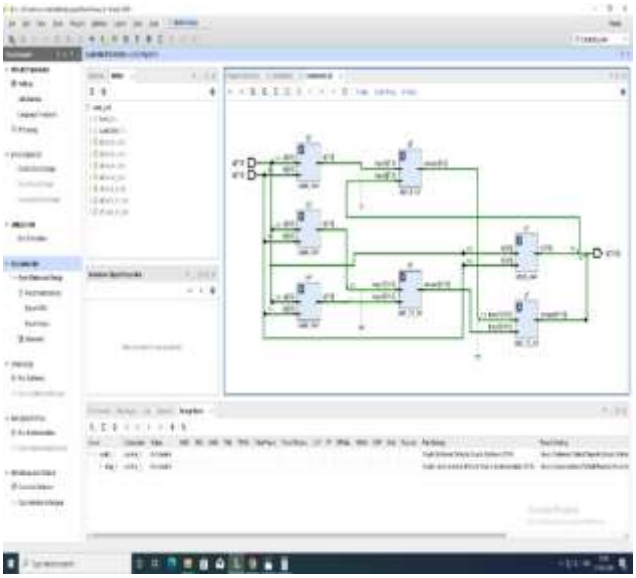

Fig.4.Synthesis report for the modified Vedic Multiplier.

The Power report and the LUT's utilization for the 8-bit Vedic Multiplier is shown below.
In this 8-bit Vedic Multiplier the static power consumption is 1%(0.486W) and the dynamic power consumption is 99% (37.684W). Coming to the LUT's utilization here 94 LUT's are utilized and 32 I/O ports are used.

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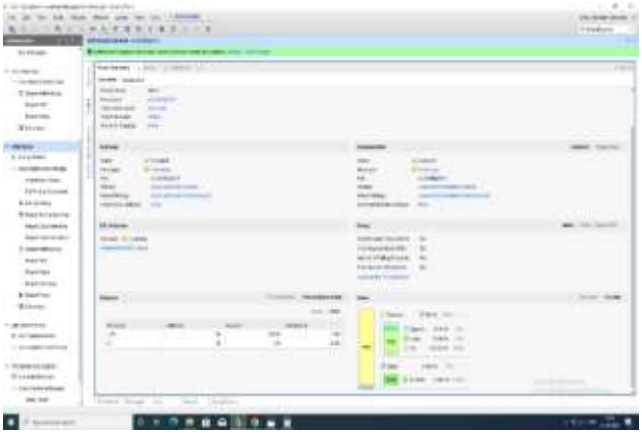
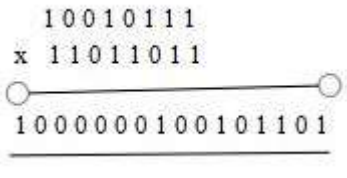


Fig.5.Power report and LUT's utilization report for the modified Vedic Multiplier.

The hardware implementation for this 8-bit Vedic Multiplier is shown below. Here we have taken an example:



The above shown example is implemented on the hardware kit , then we got the output which is shown in the figure.

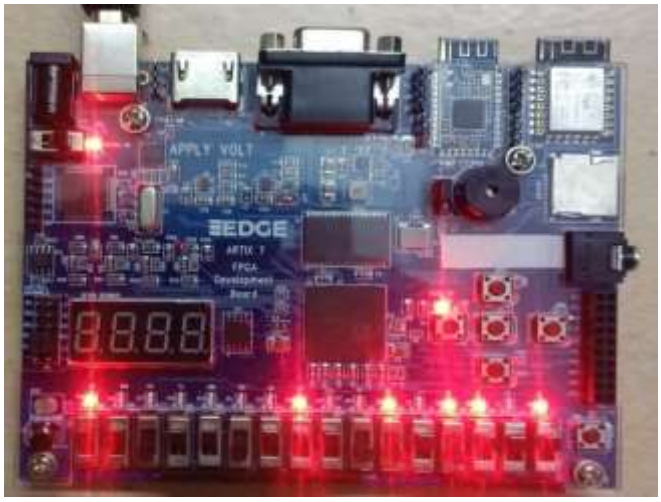


Fig.6. Hardware implementation kit for the modified Vedic Multiplier.

Table II. Vedic Multipliers using Wallace Tree Technique Delay and No. of LUT's used.

S. No	Vedic Multiplier using Wallace Tree Technique	Delay (in ns)	LUT's
1.	2-Bit	10.115	1

2.	4-Bit	15.252	7
3.	8-Bit	21.232	72
4.	16-Bit	21.401	157
5.	32-Bit	24.221	430

Table III .Modified Vedic Multiplier Delay and No. of LUT's used.

S. No	Modified Multiplier Vedic	Delay ns) (in	LUT's
1.	2-Bit	5.618	2
2.	4-Bit	6.798	16
3.	8-Bit	7.542	94
4.	16-Bit	10.928	248
5.	32-Bit	12.526	680

The above table II and table III shows the difference between the delay and no. of LUT's used in the Existing 32-Bit Vedic Multiplier and Modified 32-Bit Vedic Multiplier.

VI CONCLUSION

In order to boost operating speed, this project implements a multiplier unit. Thus, the multiplier is used as a fundamental approach for carrying out applications over a variety of processes. It is also used in cryptography to increase the security of the system. The suggested Vedic mathematics based on a Nikhilam architecture for 2,4,8,16, and 32 bit binary number system multiplication was built in addition to the Wallace Tree and Urdhva Tiriyagbhyam structures now in use. With the aid of the Xilinx ISE Tool, the many sorts of architectures included in this project were designed and implemented using the Verilog HDL language.

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